1. write a Verilog gate-level description of the circuits shown in

a. Fig.1 b. Fig.2 c. Fig.3
d. Fig.4 e. Fig.5 f. Fig.6

2. Using continuous assignment statements, write a Verilog description of the circuit shown in

a. Fig.1 b. Fig.2 c. Fig.3
d. Fig.4 e. Fig.5 f. Fig.6

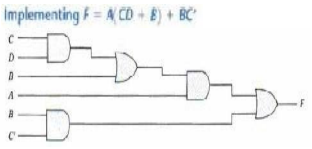

Fig.1

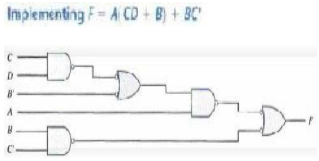

Fig.2

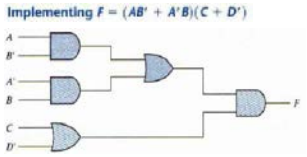

Fig.3

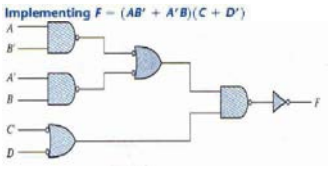

Fig.4

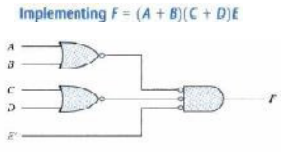

Fig.5

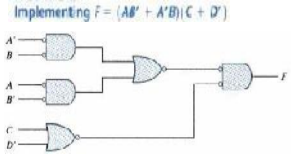

Fig.6

3. The exclusive-OR circuit of Fig.3 has gates with a delay of 4 ns for an inverter, a 8 ns delay for an AND gate, and a 10 ns delay for an OR gate. The input of the circuit goes from xy = 00 to xy = 01.

a. Determine the signals at the output of each gate from t = 0 to t = 50 ns.
b. Write a Verilog gate-level description of the circuit including the delays.
c. Write a stimulus module (i.e. a test bench) and stimulate the circuit to verify the answer in part(a).

4. Using continuous assignments, write a Verilog description of the circuit specified by the following Boolean functions:

Out_1 = (C + B)(A' + D)B'
Out_2 = (CB' + ABC + C'B)(A + D') Out_3 = C(AD + B) + BA'

Write a test bench and simulate the circuit's behavior.

5. Find the syntax errors in the following declarations (note that names for primitive gates are optional):

```
module Exmple-3(A. B. C. D. F)      //Line  1   inputs
    A,B,C,Output D,F,               //Line 2  output  B
                                    //Line 3
    and  g1(A,B.D);                 //Line 4
    not  (D,A,C),                   //Line 5
    OR  (F,B;C);                    //Line 6
endofmodule;                        //Line 7
```

6. Draw the logic diagram of the digital circuit specified by the following Verilog descripton:

a.
```
module Circuit_A(A,B,C,D,F); input
    A,B,C,D;
    output  F;
    wire   w,x,y,z,a,d;
    and   (x,B,C,d);
    and   (y,a,C);
    and   (w,z,B);
    or   (z,y,A);
    not   (a,A);
    not   (d,D); endmodule
```

b.
```
module Circuit_B(A_gtB,A_ltB,A_eqB,A0,A1,B0,B1); output
    A_gtB,A_ltB,A_eqB;
    input  A0,A1,B0,B1;
    nor   (A_gtB,A_ltB,A_eqB); or
    (A_ltB,w1,w2,w3); and
    (A_eqB,w4,w5);
    and   (w1,w6,B1);
    and   (w3,w7,B0,B1);
    not   (w6,A1);
    not   (w7,A0);
    xnor  (w4,A1,B1);
    xnor  (w5,A0,B0); endmodule
```

c.
```
module Circuit_C(output y1, input a,b, output y2);  assign y1
    = a & b;
    or (y2,a,b); endmodule
```

7. A majority logic function is a Boolean function that is equal to 1 if the majority of the variables are equal to 1,equal to 0 otherwise. Write a Verilog user-defined primitive for a four-bit majority function.

8. Simulate the behavior of Circuit_with_UDP_02467,using the stimulus waveforms shown: