1. Design a sequential circuit with two D flip-flops A and B. and one input x. When x = 0. the state of the circuit remains the same. When x = 1, the circuit goes through the state transitions from 00 to 01 to 11 to 10 back to 00, and repeats.
2. Design a one input, one output serial 2's complementer. The circuit accepts a string of bits from the input and generates the 2's complement at the output. The circuit can be reset asynchronously to start and end the operation.
3. Design a sequential circuit with two JK flip-flops A and B and two inputs E and x. If E = 0, the circuit remains in the same state regardless of the value of x. When E = 1 and x = 1, the circuit goes through the state transitions from 00 to 01 to 10 to 11 back to 00, and repeats. When E = 1 and x = 0, the circuit goes through the state transitions from 00 to 11 to 10 to 01 back to 00, and repeats.
4. A sequential circuit has three flip-flops A, B, C; one input x; and one output y. The state diagram is shown in the following figure. The circuit is to be designed by treating the unused states as don't- care conditions. Analyze the circuit obtained from the design to determine the effect of the unused states.
   (a) Use T flip-flops in the design. (b) Use JK flip-flops in the design.