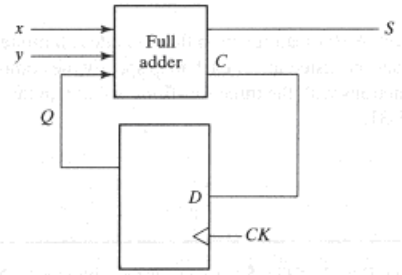
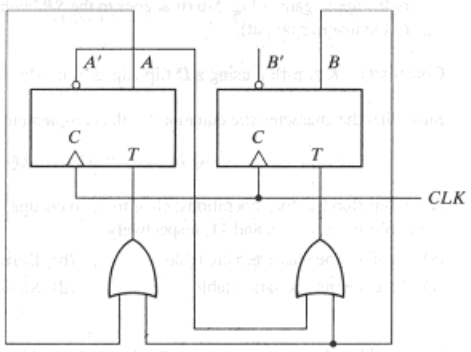
1. Construct D latch using one of the following and in each case, draw the logic diagram and verify the circuit operation.
   (a) Use NOR gates for the SR latch part and AND gates for the other two. An inverter may be needed.
   (b) Use NOR gates for all four gates. Inverters may be needed.
   (c) Use four NAND gates only (without an inverter).

2. A PN flip-flop has four operations: clear to 0, no change, complement, and set to 1, when inputs P and N are 00, 01, 10, and 11, respectively.
   (a) Tabulate the characteristic table.
   (b) Derive the characteristic equation.
   (c) Tabulate the excitation table.
   (d) Show how the PN flip-flop can be converted to a D flip-flop.
   (e) Verify your circuit using Verilog.

3. A sequential circuit has one flip-flop Q, two inputs x and y, and one output S. It consists of a full. adder circuit connected to a D flip-flop, as shown in the following figure. Derive the state table and state diagram of the sequential circuit.



4. Derive the state table and the state diagram of the sequential circuit shown in the following figure. Explain the function that the circuit performs.



5. A sequential circuit has two JK flip-flops A and B, two inputs x and y, and one output z. The flip-flop input equations and circuit output equation are:

$J_A = B\,x + B'\,y'$ $K_A = B'\,x\,y'$

$J_B = A'\,x$ $K_B = A + x\,y'$

$z = A\,x'\,y' + B\,x'\,y'$

   (a) Draw the logic diagram of the circuit.
   (b) Tabulate the state table.
   (c) Drive the state equations for A and B.
   (d) Draw the corresponding state diagram.