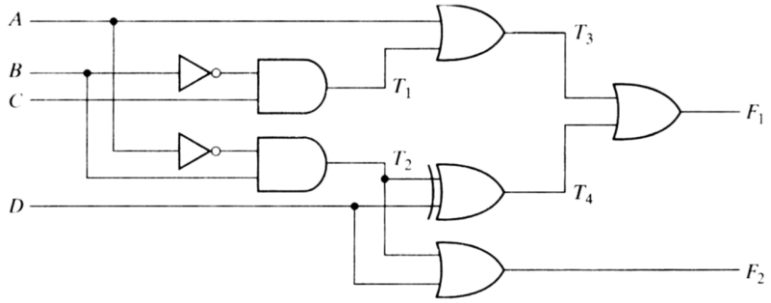
1. Consider the combinational circuit shown in the following figure:

   (a) Derive the Boolean expressions for ***T1*** through ***T4.*** Evaluate the outputs *F1* and *F2* as a function of the four inputs.

   (b) List the truth table with 16 binary combinations of the four input variables. Then list the binary values for *T1* through *T4* and outputs *F1* and *F2* in the table.

   (c) Plot the output Boolean functions obtained in part (b) on maps and show that the simplified Boolean expressions are equivalent to the ones obtained in part (a).



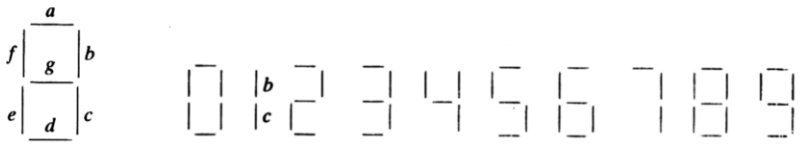
2. Design a combinational circuit with three inputs and one output. The output is 1 when the binary value of the inputs is less than 3. The output is 0 otherwise. Write down the Verilog description of this circuit using gate-level.

3. Design a combinational circuit with three inputs, x, y, and z, and three outputs, *A*, *B*, and *C*. When the binary input is 0, 1, 2, or 3, the binary output is one greater than the input. When the binary input is 4, 5, 6, or 7, the binary output is one less than the input. Write down the Verilog description of this circuit using dataflow.

4. ABCD-to-seven-segment decoder is a combinational circuit that converts a decimal digit in BCD to an appropriate code for the selection of segments in a display indicator used for displaying the decimal digit in a familiar form. The seven outputs of the decoder (a, *b, c, d, e, f,* g) select the corresponding segments in the display, as shown in the following Figure.

   (a). The numeric display chosen to represent the decimal digit is shown in the following Figure.

   (b). Design the BCD-to-seven-segment decoder using a minimum number of gates. The six invalid combinations should result in a blank display.



(a) Segment designation (b) Numerical designation for display

FIGURE P4-9

5. Design a 4-bit combinational circuit incrementer using four half-adders. (A circuit that adds one to a 4-bit binary number.)

6. (a) Design a half-subtractor circuit with inputs x and y and outputs *D* and *B.* The circuit subtracts the bits x - y and places the difference in *D* and the borrow in *B*

   (b) Design a full-subtractor circuit with three inputs x y, z and two outputs D and *B.* The circuit subtracts x - y - z, where is the input borrow, *B* is the output borrow, and 0 is the difference.

   (c) Write verilog description of full-subtractor using gate level hierarchical description.

7. The adder-subtractor circuit has the following values for mode input M and data inputs *A* and *B.* In each case, determine the values of the four SUM outputs, the carry *C,* and overflow *V*

	M	*A*	*B*
(a)	0	0111	0110
(b)	0	1000	1001
(c)	1	1100	1000
(d)	1	0101	1010
(e)	1	0000	0001

8. (a). Design a combinational circuit that generates the 9's complement of a BCD digit.

   (b). Construct a BCD adder-subtractor circuit, using the BCD adder and the 9's cornplementer of (a). Use block diagrams for the components.

9. Design a binary multiplier that multiplies two 4-bit numbers. Use AND gates and binary adders.

10. Design a combinational circuit that compares two 4-bit numbers to check if they are equal. Circuit output is equal to I if the two numbers are equal and 0 otherwise.

11. Draw the logic diagram of a 2-to-4-line decoder using NOR gates only. Include an enable input.

12. Construct a 5-to-32-line decoder with four 3-to-8-line decoders with enable and a 2-to-4- decoder. Use block diagrams for the components.

13. A combinational circuit is specified by the following three Boolean functions:

$$F_1(A, B, C) = \sum(2, 4, 7)$$
$$F_2(A, B, C) = \sum(0, 3)$$
$$F_3(A, B, C) = \sum(0, 2, 3, 4, 7)$$

Implement the circuit with a decoder constructed with NAND gates connected to the decoder outputs. Use a block diagram for the decoder. Minimize the number of inputs in the external gates.

14. Specify the truth table of an octal-to-binary priority encoder. Provide an output *V* to indicate at least one of the inputs is present. The input with the highest subscript number has the highest priority. What will be the value of the four outputs if inputs *D5* and *D3* are 1 at the same time?

15. Construct a 16 × 1 multiplexer with two 8 × I and one 2 × 1 multiplexers. Use block diagram.

16. Implement the following Boolean function with a multiplexer:

$$F(A, B, C, D) = \sum(0, 1, 3, 4, 8, 9, 15)$$

17. An 8 × I multiplexer has inputs *A, B,* and C connected to the selection inputs S2, S1 and S0, respectively. The data inputs *1* through *I,* are as follows: $1_1 = 1_2 = 1_7 = 0$; $1_3 = 1_5 = 1$; $I_0 = I_4 = D$; and $I_6 = D'$. Determine the Boolean function that the multiplexer implements.

18. *Implement* the *following* Boolean *function with a* 4 X 1 multiplexer *and external* gates. *Connect* inputs *A* and *B* to the selection lines. The input requirements for the four data lines will be a function of variables *C* and *D.*

$$F\ (A, B, C, D) = \Sigma(1,3,4,11, 12, 13,14,15)$$