

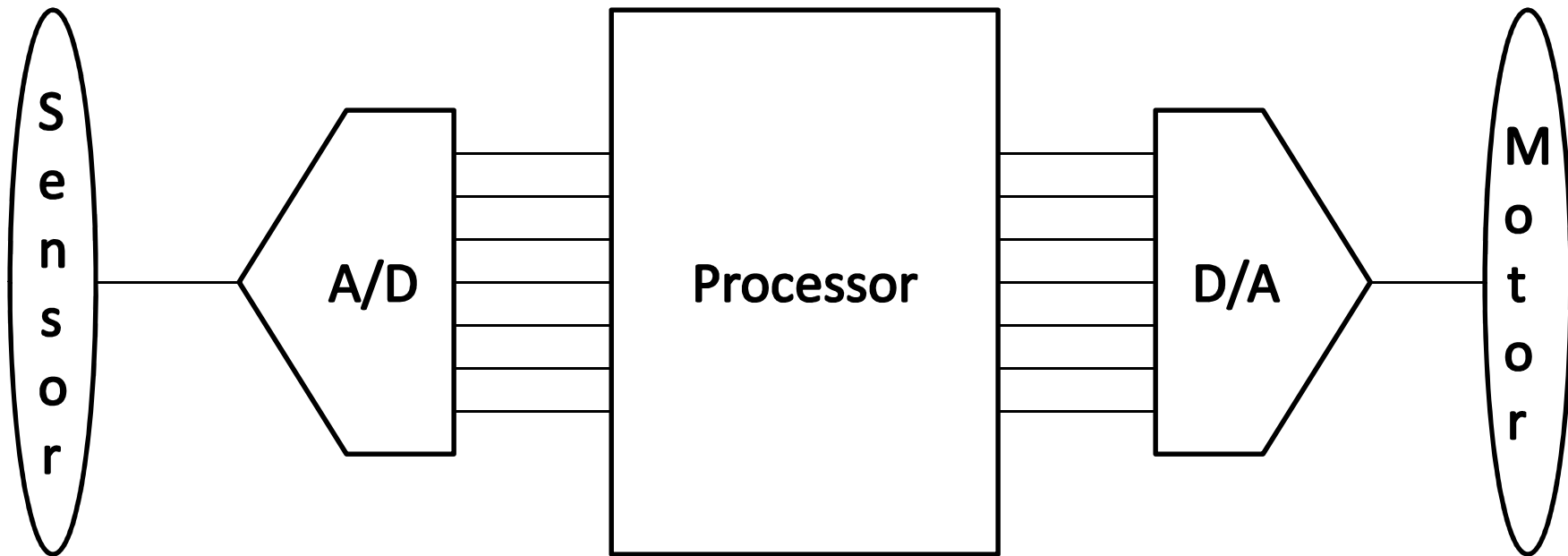


Faculty of Engineering

MCT242: Electronic Instrumentation

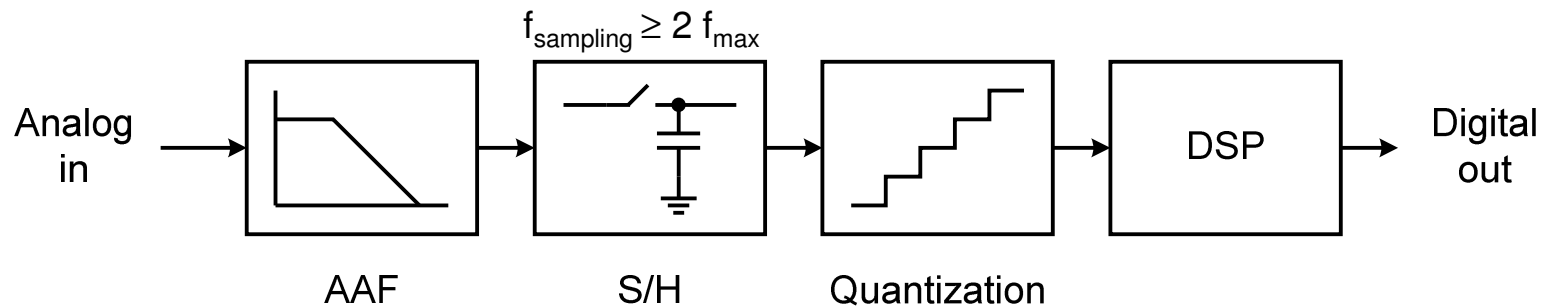
**Lecture 9:
Analog to Digital Converters**

A/D and D/A Conversion

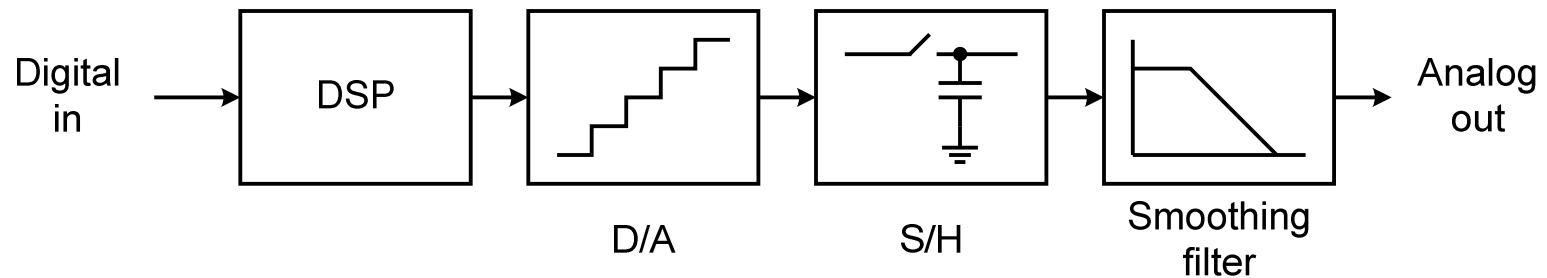


A/D and D/A Conversion

A/D Conversion

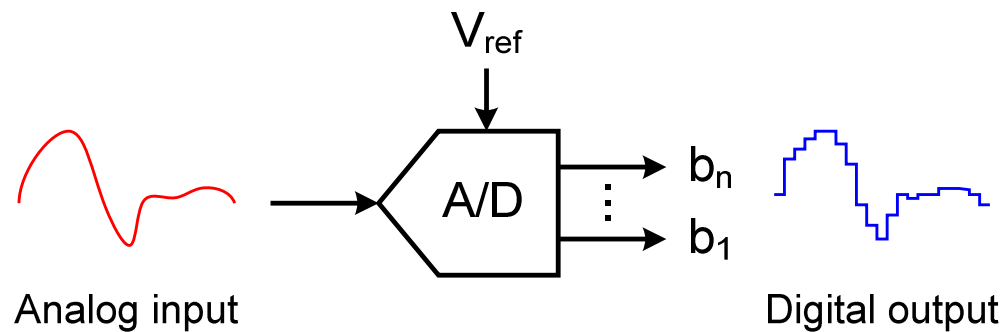


D/A Conversion



A/D Converters

Quantization



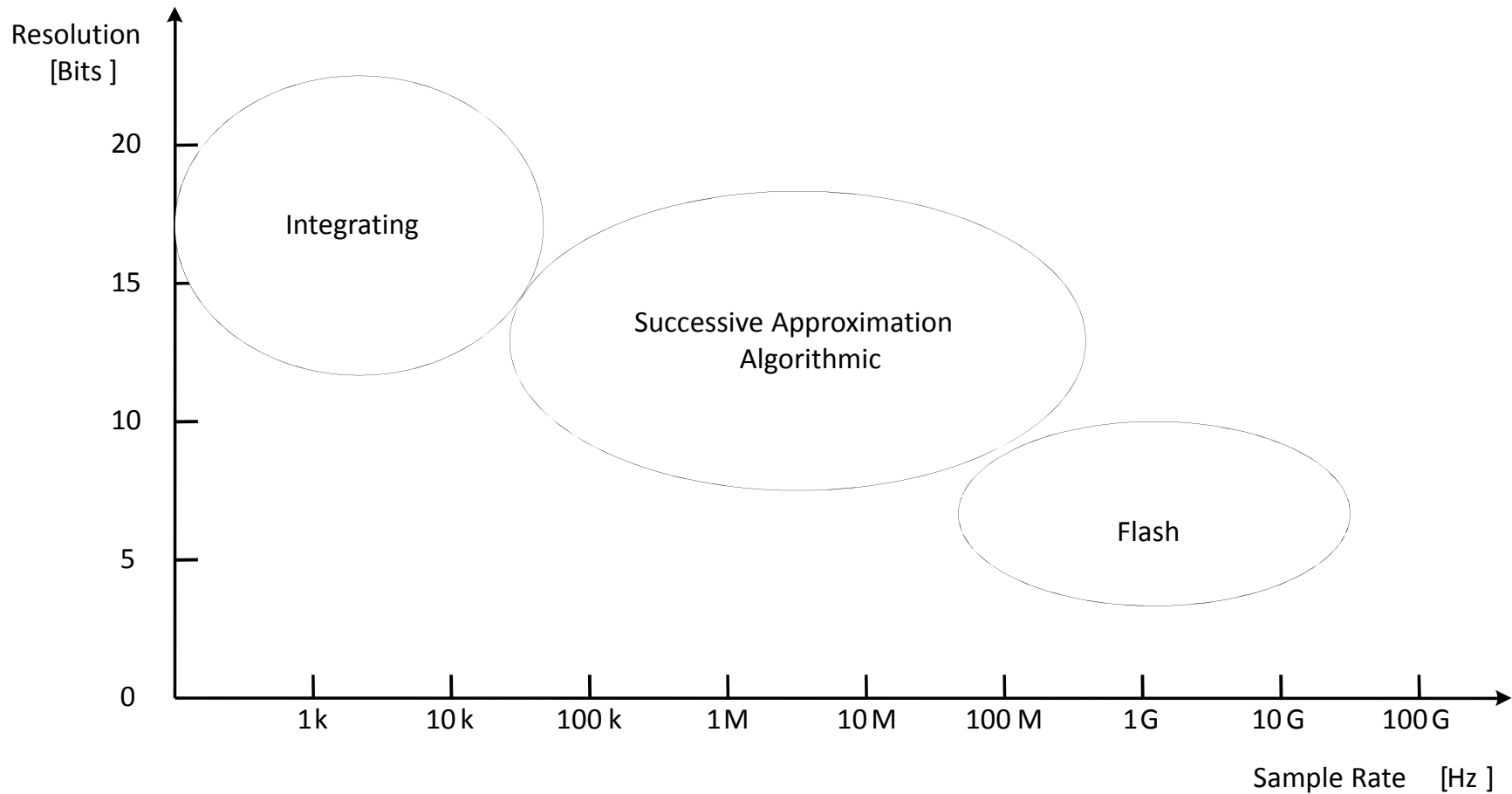
Division :
$$D_{out} = \left\lfloor 2^N \cdot \frac{V_{in}}{V_{FS}} \right\rfloor$$

- Quantization = division + normalization + truncation
- Full-scale range (V_{FS}) is determined by V_{ref}

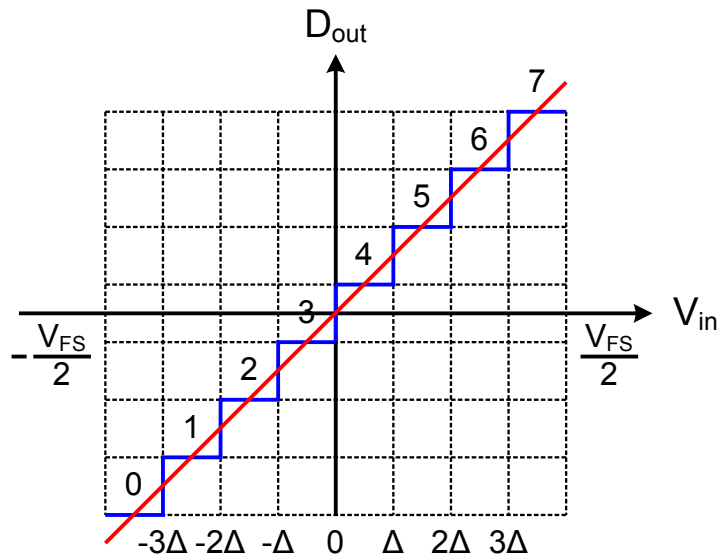
Nyquist-Rate ADC (N-Bit, Binary)

- Word-at-a-time (1 step)[†] ← fast
 - Flash
- Level-at-a-time (2^N steps) ← slow
 - Integrating (Serial)
- Bit-at-a-time (N steps) ← medium
 - Successive approximation

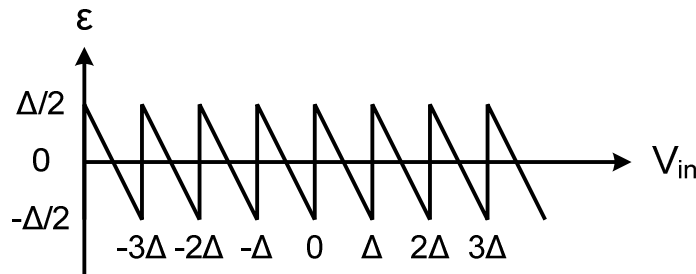
Accuracy-Speed Tradeoff



Quantization Error



$N = 3$



$$\Delta = \frac{V_{FS}}{2^N} = \text{LSB}$$

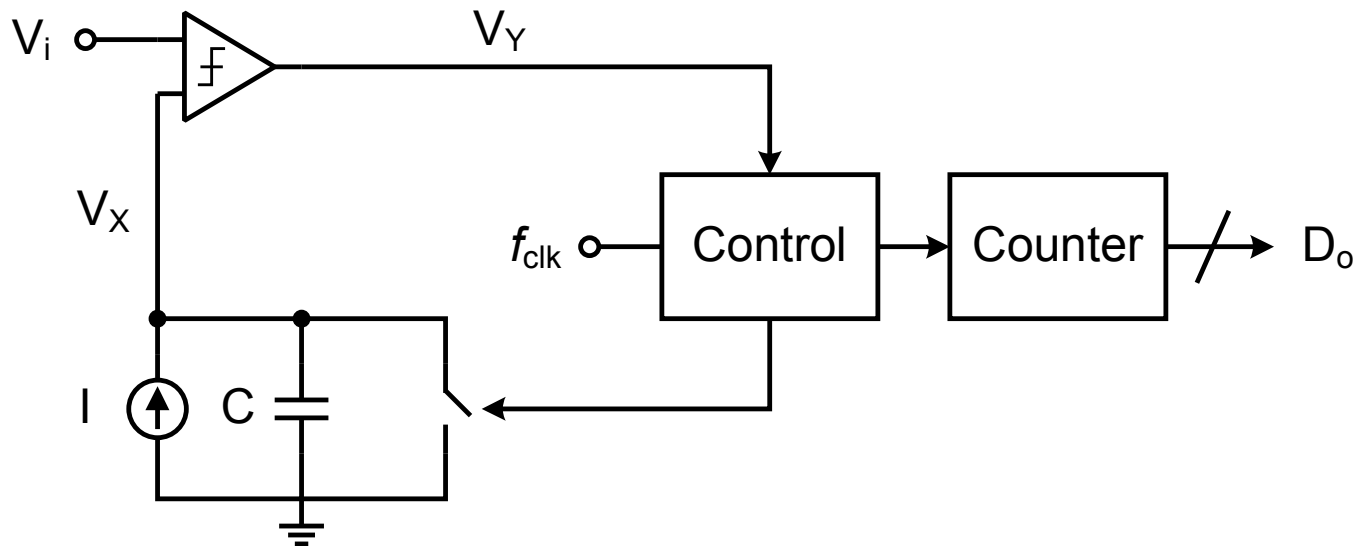
$$V_{in} \in [0, V_{FS}]$$

$$\varepsilon = D_{out} \Delta - V_{in} = D_{out} \left(\frac{V_{FS}}{2^N} \right) - V_{in}$$

$$-\frac{\Delta}{2} \leq \varepsilon \leq \frac{\Delta}{2}$$

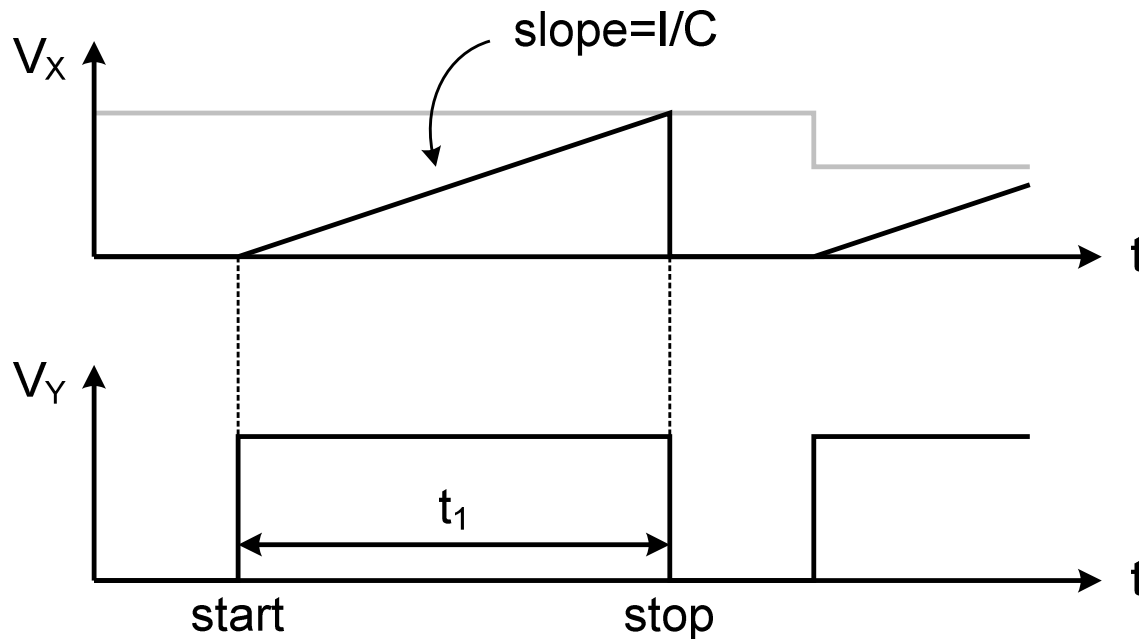
“Random” quantization error is usually regarded as noise

Single-Slope Integrating ADC



- Sampled-and-held input (V_i)
- Counter keeps counting until comparator output toggles
- Simple, inherently monotonic, but very slow ($2^N \cdot T_{clk}$ /sample)

Single-Slope Integrating ADC



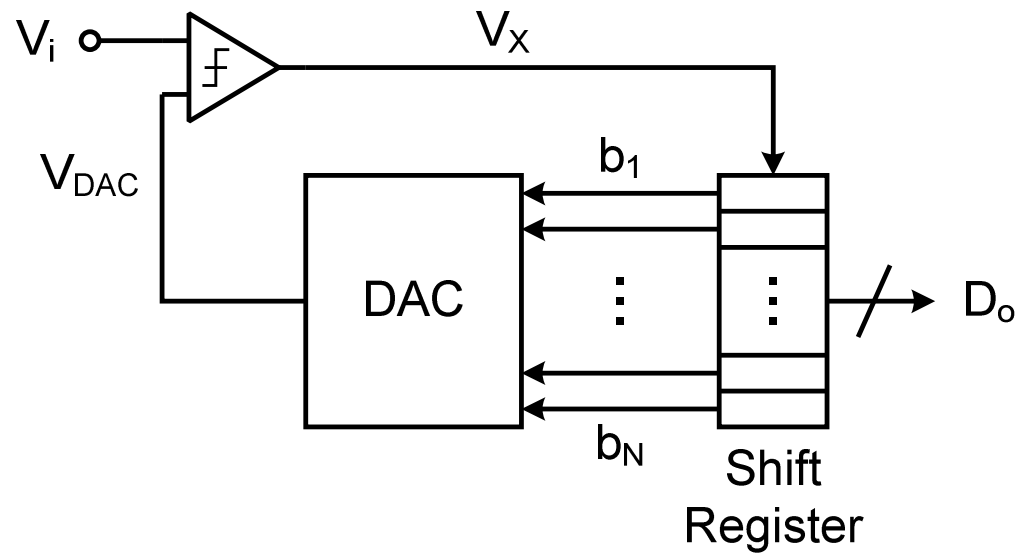
$$V_i = \frac{I}{C} \cdot t_1, \quad D_o = \left\lfloor \frac{t_1}{T_{\text{clk}}} \right\rfloor$$

$$\Rightarrow D_o = \left\lfloor \frac{V_i}{\left(\frac{I \cdot T_{\text{clk}}}{C} \right)} \right\rfloor,$$

$$\text{LSB} = \frac{I \cdot T_{\text{clk}}}{C}$$

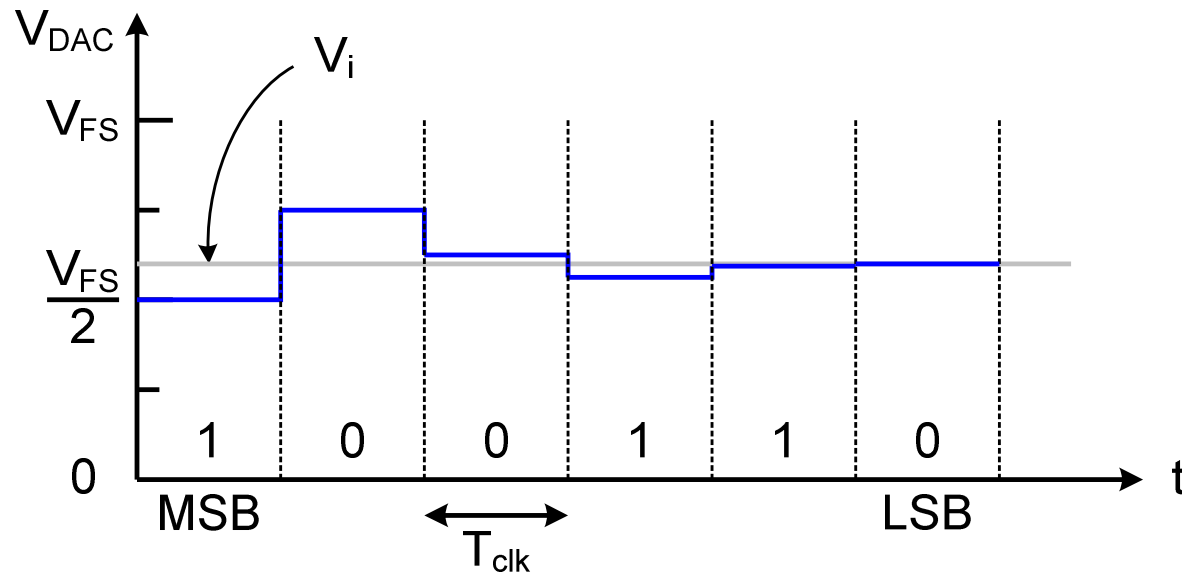
- INL depends on the linearity of the ramp signal
- Precision capacitor (C), current source (I), and clock (T_{clk}) required
- Comparator must handle wide input range of $[0, V_{\text{FS}}]$

Successive Approximation ADC



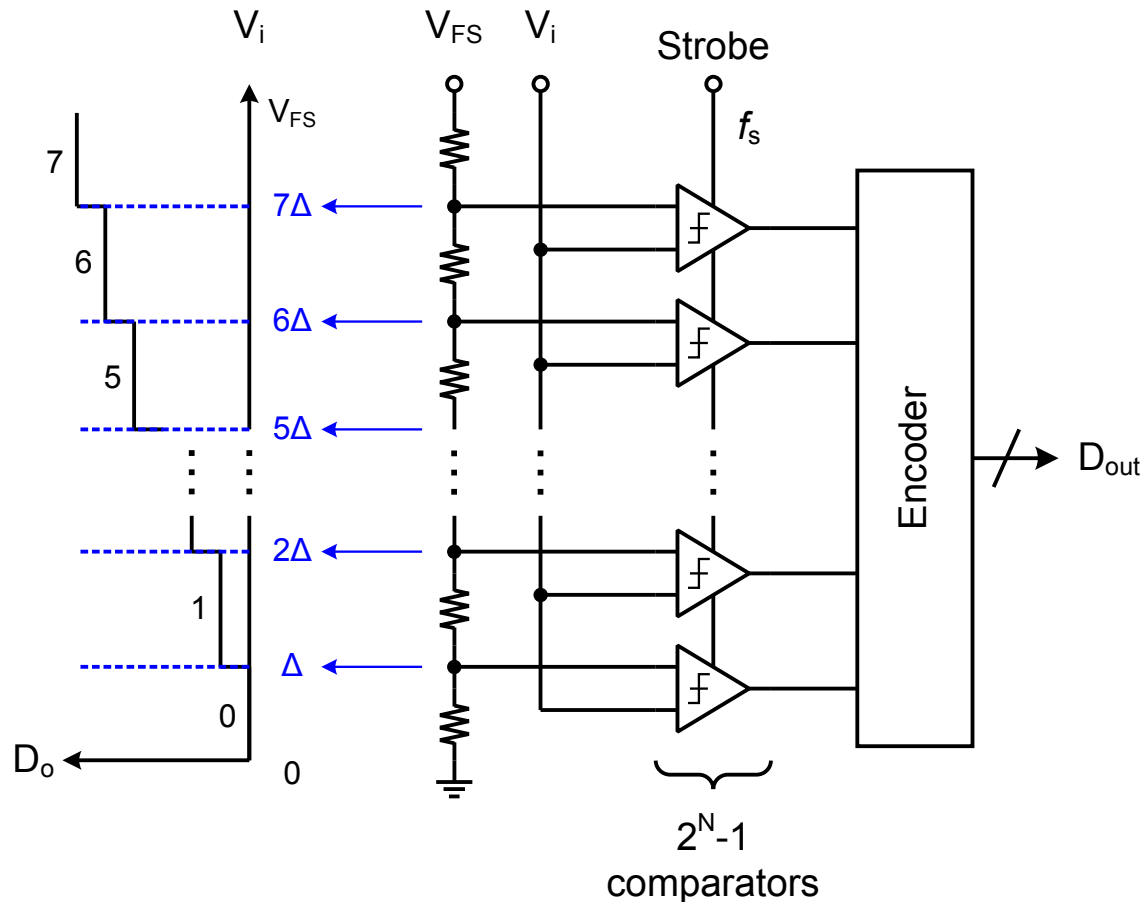
- Binary search algorithm $\rightarrow N \cdot T_{clk}$ to complete N bits
- Conversion speed is limited by comparator, DAC, and digital logic (successive approximation register or SAR)

Binary Search Algorithm



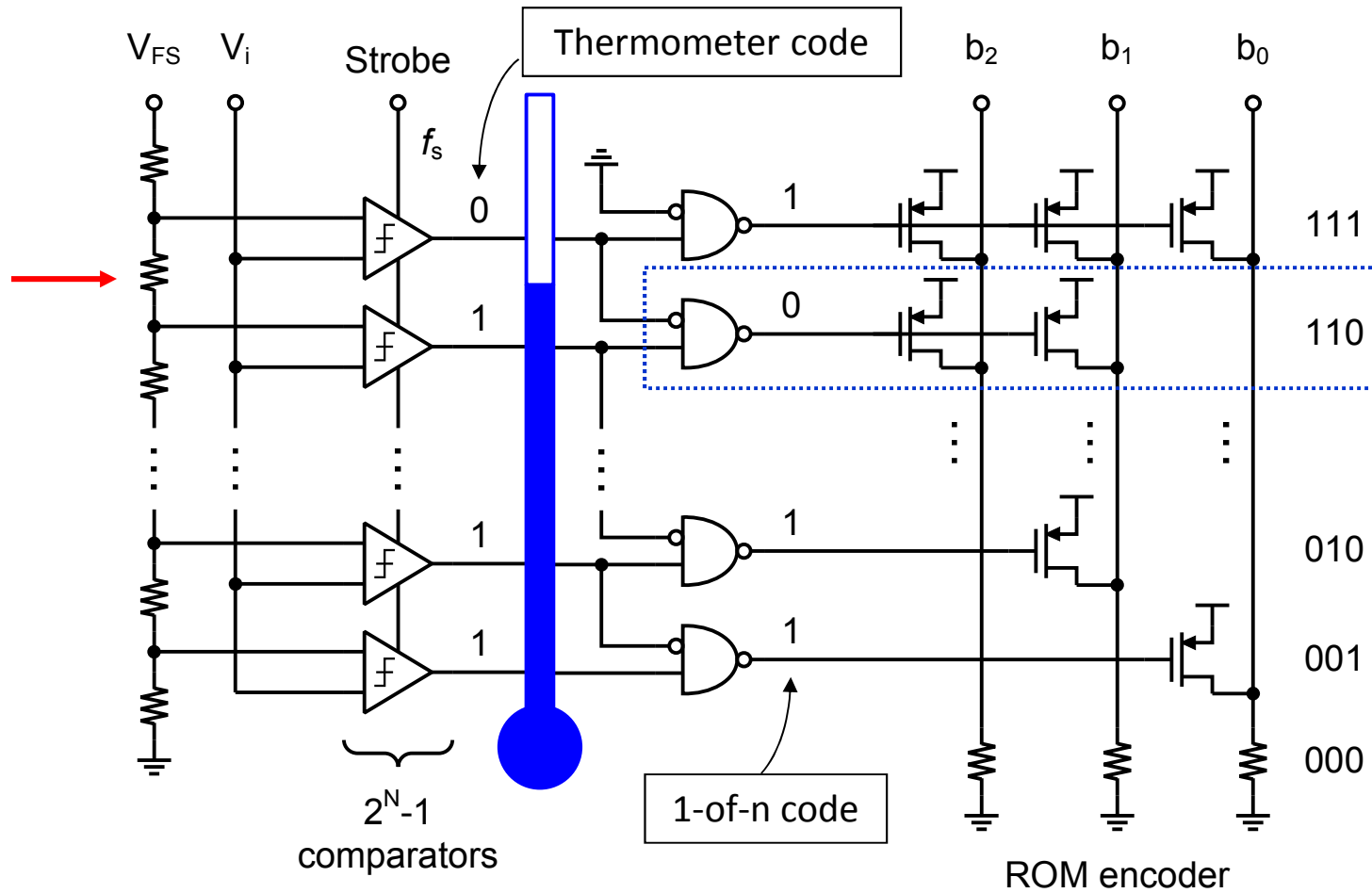
- DAC output gradually approaches the input voltage
- Comparator differential input gradually approaches zero

Flash ADC Architecture



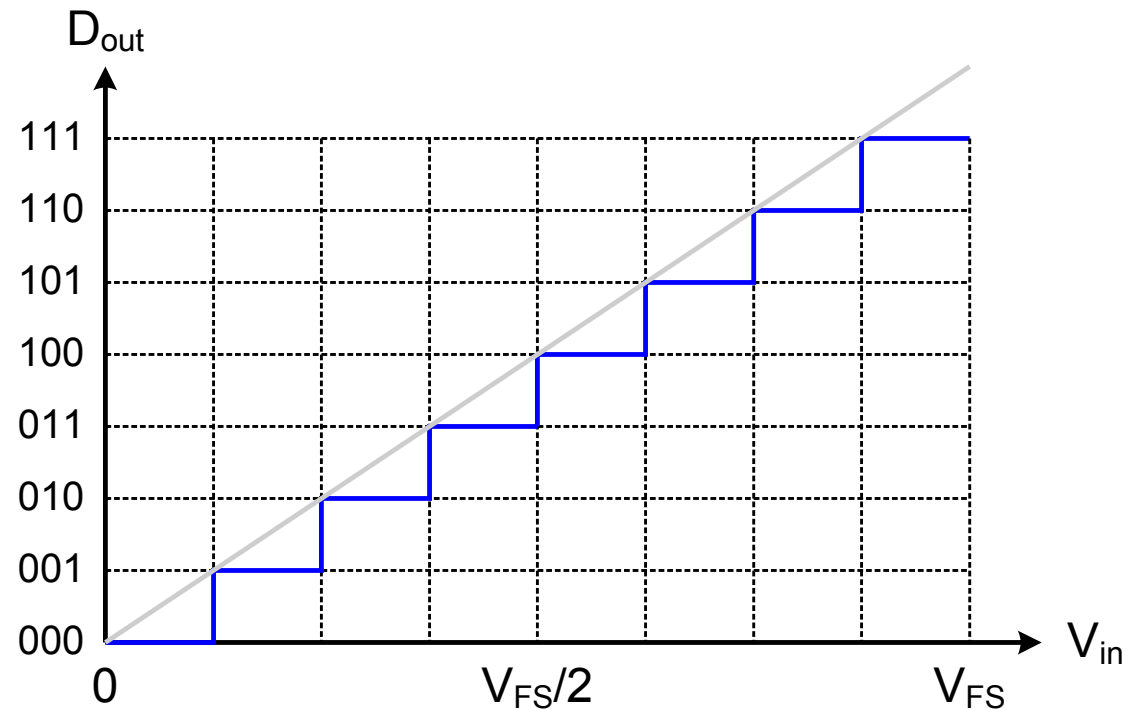
- Reference ladder consists of 2^N equal size resistors
- Input is compared to $2^N - 1$ reference voltages
- Massive parallelism
- Very fast ADC architecture
- Latency = $1 T = 1/f_s$
- Throughput = f_s
- Complexity = 2^N

Thermometer Code



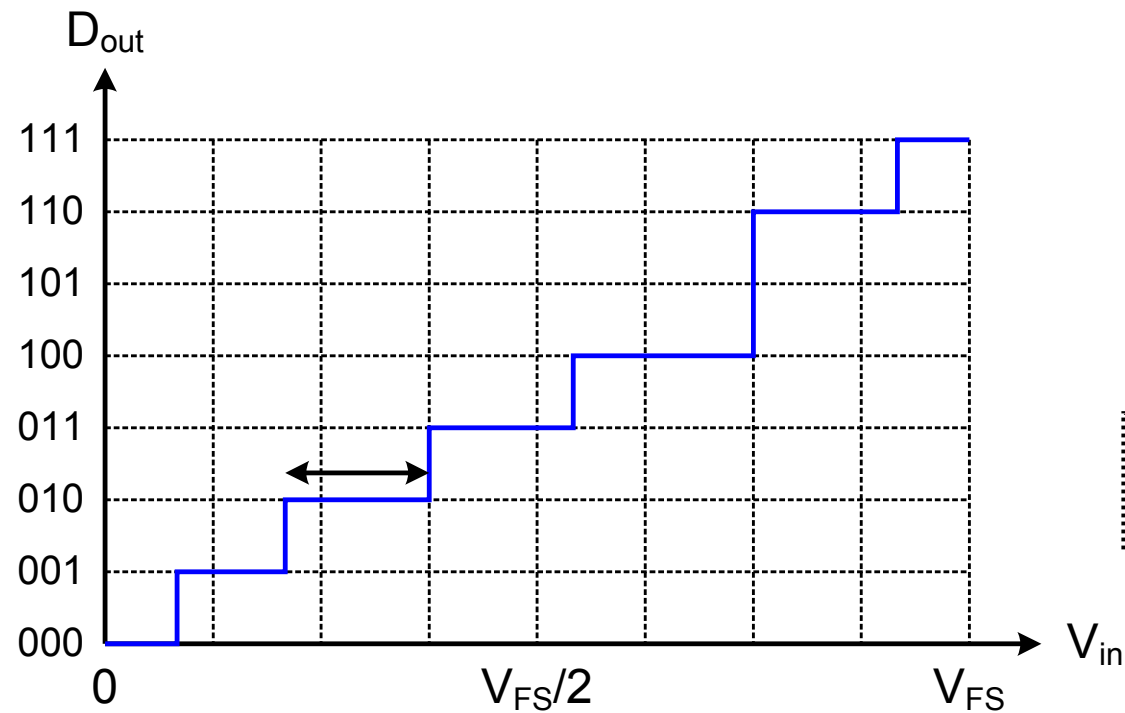
Static Performance of ADC

Ideal ADC Transfer Characteristic



Note the systematic offset! (floor, ceiling, and round)

DNL and Missing Code

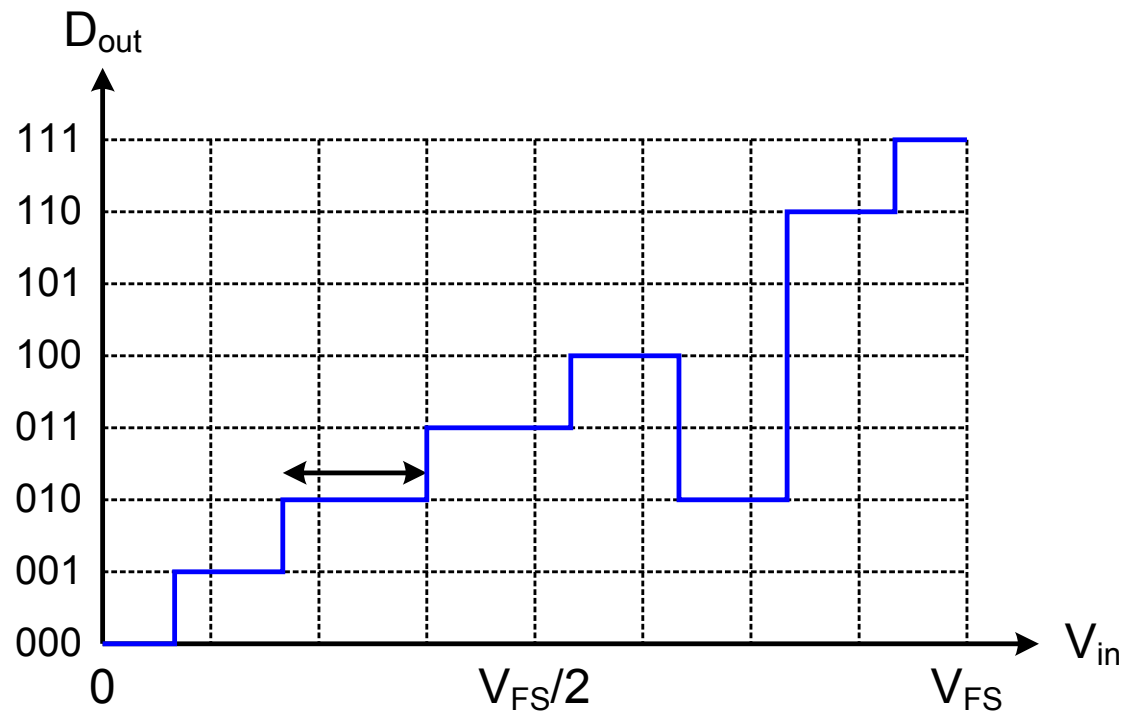


- DNL = ?

$$DNL_i = \frac{i^{\text{th}} \text{ Step Size} - \Delta}{\Delta}$$

DNL = deviation of an input step width from 1 LSB ($= V_{FS}/2^N = \Delta$)

DNL and Nonmonotonicity



DNL = deviation of an input step width from 1 LSB ($= V_{FS}/2^N = \Delta$)