ECE421: Electronics for Instrumentation

Lecture #3: Review on MEMS-IC Fabrication Processes

Mostafa Soliman, Ph.D.

Outline

- Basic MEMS Processes
- Front-End Processes
- Back-End Processes

Basic MEMS Processes

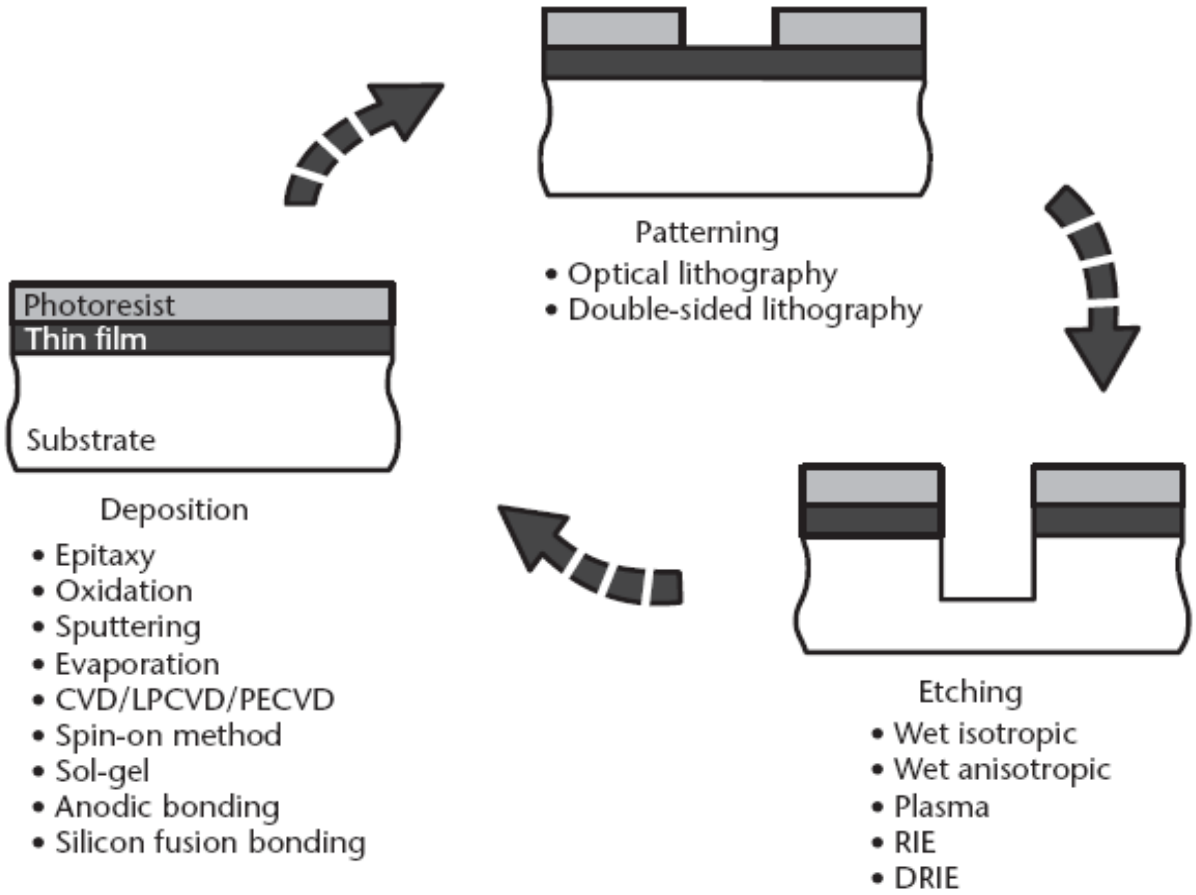
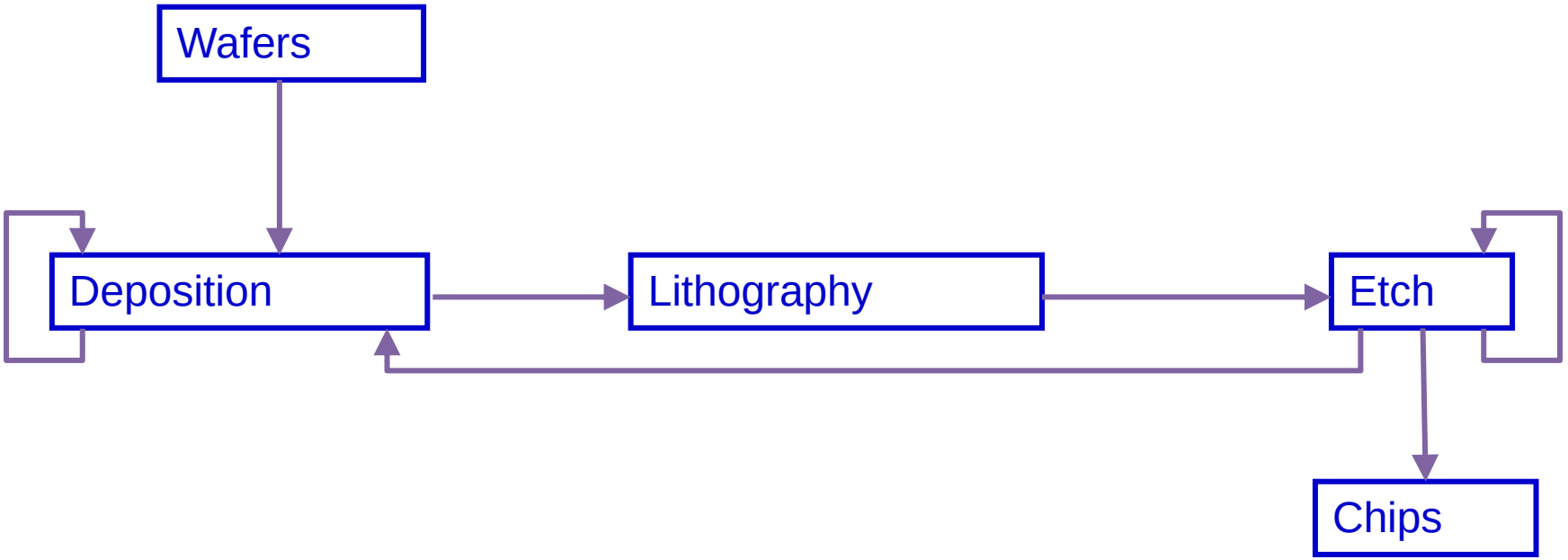


Figure 3.1 Illustration of the basic process flow in micromachining: Layers are deposited; photoresist is lithographically patterned and then used as a mask to etch the underlying materials. The process is repeated until completion of the microstructure.

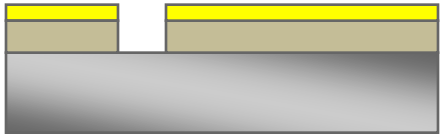
Basic MEMS Processes



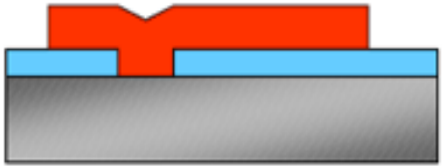
Basic MEMS Process, surface:

1- Si Substrate

3- Photo resist **deposition**

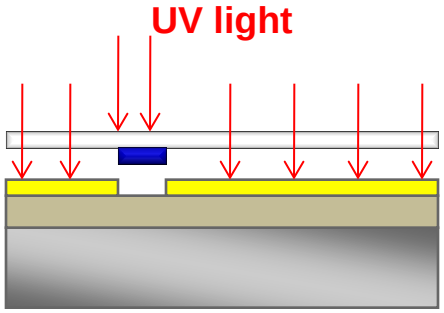


5- Sacrificial layer **etching**



7- Structural material **deposition and patterning**

2- Sacrificial layer **deposition**



4- **Photolithography (Patterning)**

6- Photo resist stripping (**etching**)

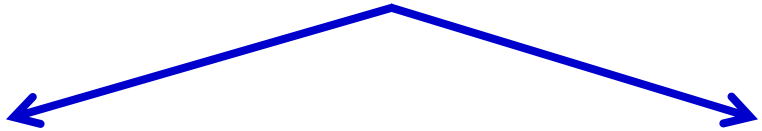
8- Sacrificial material **etching**

Materials

- Single crystal silicon – SCS
  - Anisotropic crystal
  - Semiconductor, great heat conductor
- Silicon dioxide – SiO_2
  - Excellent thermal and electrical insulator
  - Thermal oxide, LTO, PSG: different names for different deposition conditions and methods
- Silicon nitride – Si_3N_4
  - Excellent electrical insulator
- Aluminum – Al
  - Metal – excellent thermal and electrical conductor

Front-End Processes

Fabrication Processes, Micromachining



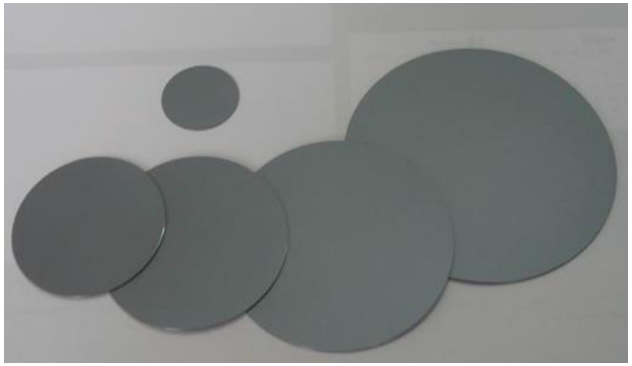
Wafer level processes	Pattern transfer
Silicon wafers	Photoresist
Wafer cleaning	Photolithography
Oxidation of silicon	Mask polarity
Doping	
Thin film deposition	
Etching	
Electrodeposition (Elctroplating)	

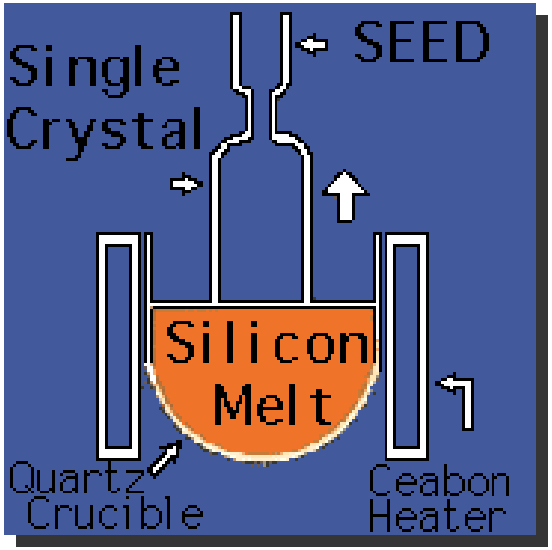
Silicon Wafers

- MEMS devices are either built into a substrate (bulk micromachining) or on a substrate (surface micromachining).
- MEMS fabrication processes start with a substrate, or a wafer.
- Silicon wafers are used in most cases as substrates for MEMS devices.
- Wafers are created by cutting the silicon ingot to thin wafers with variable thickness as desired.

Silicon ingots

Unpolished
Si wafers

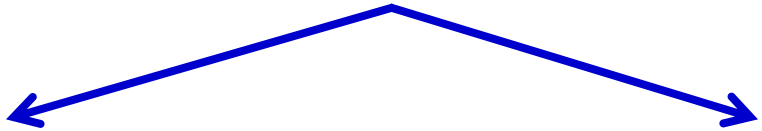




Czochralski furnace

Polished Si wafer

Fabrication Processes, Micromachining



Wafer level processes	Pattern transfer
Silicon wafers	Photoresist
Wafer cleaning	Photolithography
Oxidation of silicon	Mask polarity
Doping	
Thin film deposition	
Etching	
Electrodeposition (Elctroplating)	

Wafer Cleaning

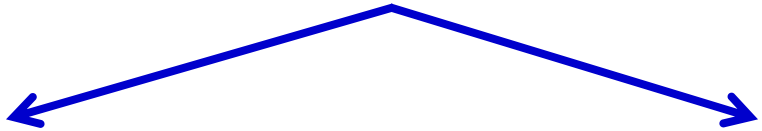
- It is necessary to clean the substrate's surface before proceeding with the micromachining.
- The **RCA cleaning** is a standard set of wafer cleaning steps which needs to be performed before high temp processing steps, like film deposition, oxidation, … etc.
- RCA cleaning includes the following steps:
  - Removal of the organic contaminants (Organic Clean)
  - Removal of thin oxide layer (Oxide Strip)
  - Removal of ionic contamination (Ionic Clean)
- The wafers are prepared by soaking them in DI water, distilled water, then performing the RCA clean as follows:

1- **Removal of all organic coatings in a strong oxidant**, such as a 7:3 mixture of concentrated sulfuric acid and hydrogen peroxide. Then organic residues are removed in a 5:1:1 mixture of water (H_2O), hydrogen peroxide (H_2O_2), and ammonium hydroxide (NH_4OH) at 80°C.

2- **Oxide removal from the first step by immersing the wafer a dilute (1:50) Hydrofluoric acid (HF)** at 25 °C to etch, or to remove or to strip, this thin oxide layer. *Note that* ***oxide is an insulator.***

3- The third and last step is performed with a 1:1:6 solution of hydrochloric acid (HCl) + hydrogen peroxide (H_2O_2) + water (H_2O) at 75 or 80 °C. This treatment **effectively removes the remaining traces of ionic contaminants.**

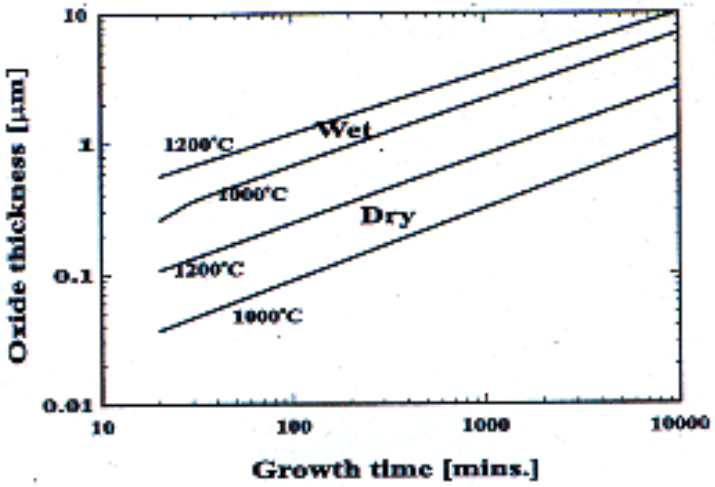
Fabrication Processes, Micromachining



Wafer level processes	Pattern transfer
Silicon wafers	Photoresist
Wafer cleaning	Photolithography
Oxidation of silicon	Mask polarity
Doping	
Thin film deposition	
Etching	
Electrodeposition (Elctroplating)	

Oxidation of Silicon

- Oxidation is one of the basic steps in the silicon processing, IC microelectronics and MEMS.
- Silicon oxidizes at room temperature in a normal atmosphere. However, this oxidation is only a few atoms thick with very low quality.
- Oxidation of silicon occurs at high temperature, usually above 800°C. The oxidation rate of silicon can be seen below.
- This gives two temperatures, 1000°C and 1200°C. As would be expected, the higher temperature yields a thicker oxide.
- This figure also shows two types of oxidation, **wet** and **dry**.
- With the **wet oxidation**, the gas is passed through a bubbler before entering the furnace. This added humidity results in a *faster oxidation* and *thick oxide films although the density and the purity of the oxide are usually low*.

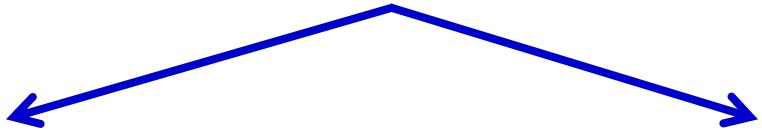


Oxidation of Silicon, *cont.*

- In **dry (or thermal) oxidation**, pure oxygen is used as the oxidant, flowed through the oxidation furnace. The oxidation rate depends on the arrival of oxygen at the silicon-oxide interface. The oxygen must diffuse through the oxide to reach this interface (oxide-silicon interface), so as the oxide gets thicker, this arrival rate decreases.
- As a result, a bare silicon wafer grows oxide relatively quickly, but an already-oxidized wafer, subjected to the same conditions, adds relatively little additional oxide.
- Oxidation rate is very *slow* in thermal oxidation, but on the other hand it is *more dense and it has better quality and purity* than wet oxidation.
- ~2-3um films are maximum practical.

A layer of Silicon Dioxide (SiO_2) will result from both thermal and wet oxidation of silicon processes on top of the Si wafer.

Fabrication Processes, Micromachining



Wafer level processes	Pattern transfer
Silicon wafers	Photoresist
Wafer cleaning	Photolithography
Oxidation of silicon	Mask polarity
Doping	
Thin film deposition	
Etching	
Electrodeposition (Elctroplating)	

Doping of Silicon

- The basic silicon wafer is either *n*-type or *p-type* doped. Additional steps are used to define differently doped regions in the substrate. This can be performed by either *diffusion* or *ion implantation*.

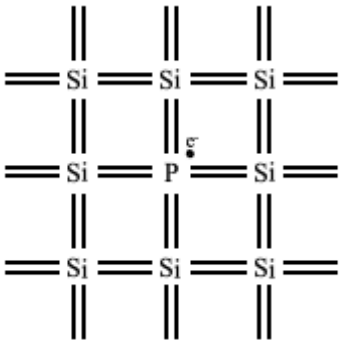
Diffusion:

Diffusion is a process in which the wafers are subjected to an atmosphere containing the desired dopant at a high temperature. The most commonly used dopants are phosphorus oxychloride ($POCL_3$) for phosphorus doping (*n*-type) and boron nitride (BN) for boron doping (*p*-type).

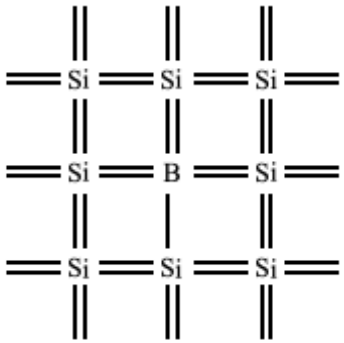
Ion Implantation:

The dopant ions are accelerated toward the wafers with energy sufficient to implement them into the wafer. The depth of the implantation is dependent upon the ion type and the energy. The most commonly used dopants are boron for p-type doping and arsenic or phosphorus for n-type doping.

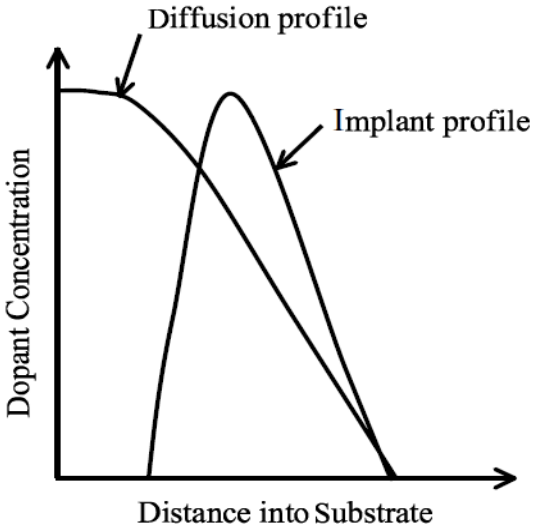
➔ Majority carriers in n-type wafers are electrons (-ve charges).
➔ Majority carriers in p-type wafers are holes (+ve charges).



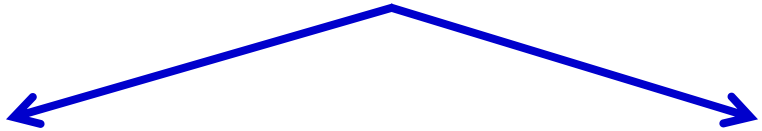
(a) n-type semiconductor with phosphorus doping



(b) p-type semiconductor with boron doping



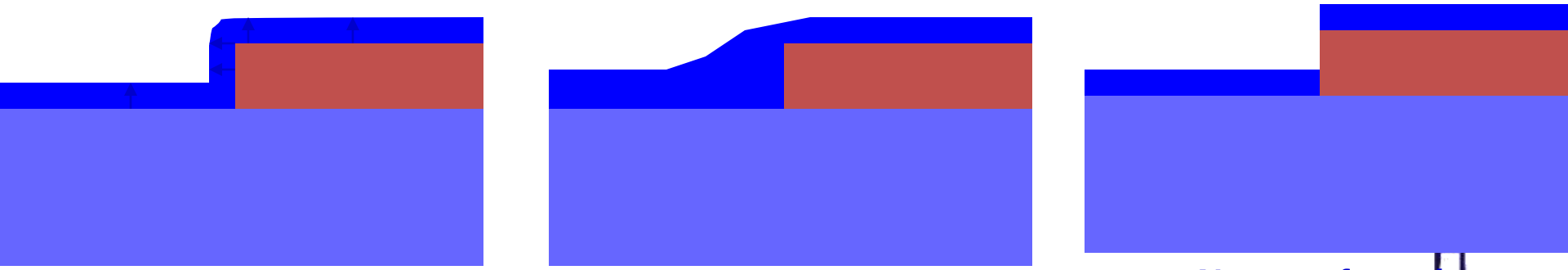
Fabrication Processes, Micromachining



Wafer level processes	Pattern transfer
Silicon wafers	Photoresist
Wafer cleaning	Photolithography
Oxidation of silicon	Mask polarity
Doping	
Thin film deposition	
Etching	
Electrodeposition (Elctroplating)	

Thin Film Deposition

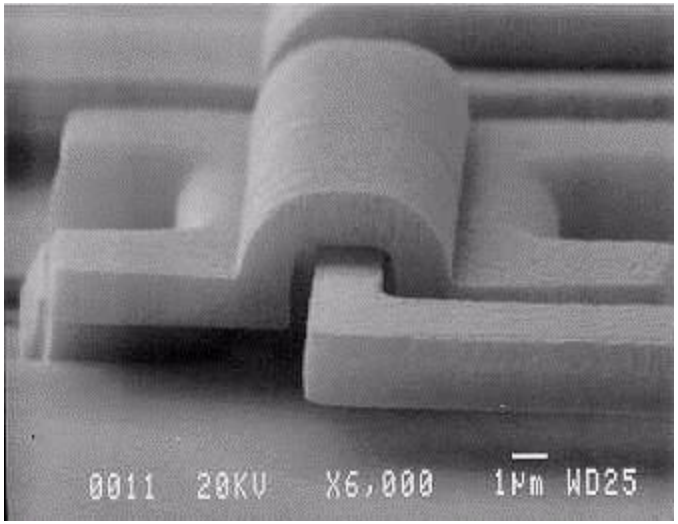
- For a number of MEMS applications, additional thin films are required to be deposited on the surface of the substrate.
- Deposited films could be metals (gold, cupper, chrome, … etc) or insulators (silicon dioxide, silicon nitride), or polysilicon.
- Two deposition methods are used, Physical Vapor Deposition (PVD) and Chemical Vapor Deposition (CVD).
- **Deposition issues, conformality:**
- A *conformal* coating covers all surfaces with a uniform depth
- A *planarizing* coating tends to reduce the vertical step height of the cross-section
- A *non-conformal* coating deposits more on top surfaces than side surfaces



Conformal **Planarizing** **Non-conformal**

Thin Film Deposition

An example of conformal deposition



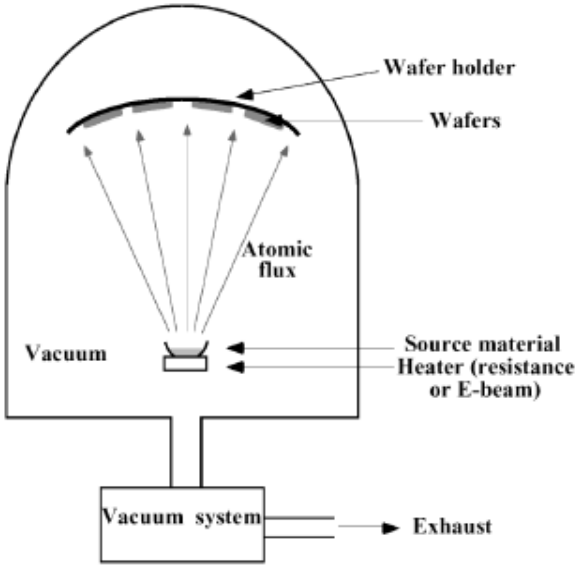
(1) Physical Vapor Deposition (PVD):

- PVD does not require a chemical reaction to deposit a thin film layer on a Si wafer.
- Conductors and insulators can be deposited using this method.
- There are 2 different processes for PVD, **Evaporation** and **Sputtering**.

Thin Film Deposition, PVD:

a) Evaporation:

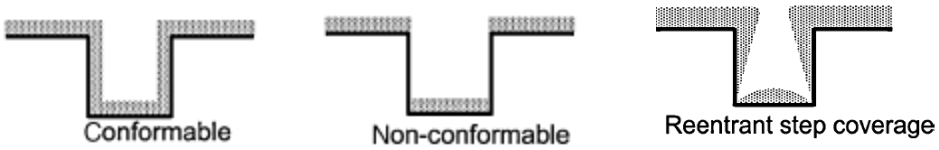
- It is the process of evaporating of a material due to very low pressure at elevated temperatures.
- The evaporator chamber consist of:
  - High vacuum chamber with an associated pumping system.
  - Crucible containing the material will be deposited with an associated heating system (resistive heating, inductive heating, or electron beam heating).
  - Wafer support structure for holding the samples will be coated.

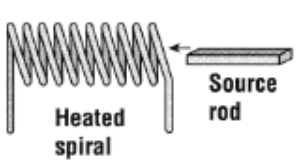


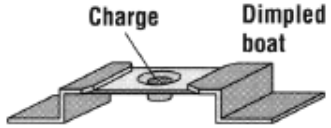
- Evaporation is a "**line of sight**" deposition phenomena from the molten material source to the wafer.

(It is a directional film deposition method).

- Step coverage issue, where sidewall are not covered with deposited material





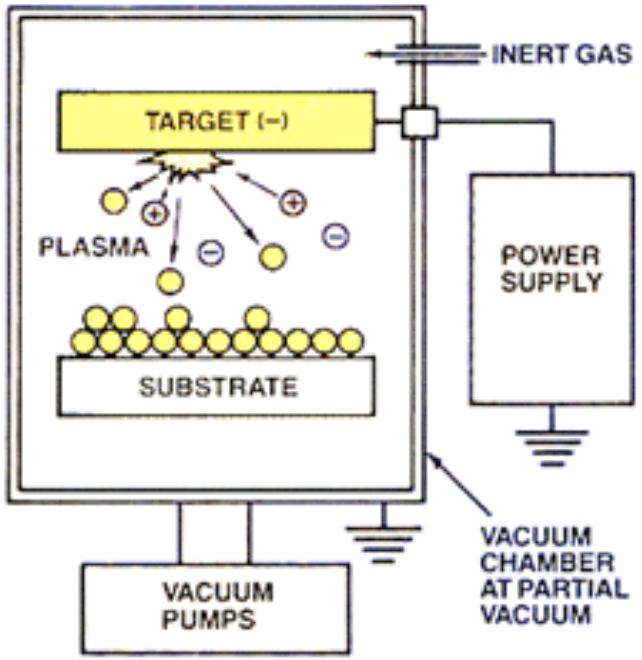


Materials: Aluminum (Al), Chrome (Cr), Si, Gold (Au), Tungsten (W), Titanium (Ti),.

Thin Film Deposition, PVD:

b) Sputtering:

- **Inert gas ions (Ar or He)** are highly accelerated toward the target, which contains the material to be deposited.
- The inert gas must be of a high atomic weight, like argon.
- The inert gas atoms are energized enough to eject the surface atoms from the target due to the impact.
- The ejected atoms from the surface are directed toward the wafer's surface to be deposited on it.
- Sputtering takes place in a low-pressure gas environment.
- It is less directional than evaporation (**better step coverage**).
- It can achieve much higher deposition rates.
- Sputtering can also be used with non-metallic targets.
- Some specialty materials, such as the piezoelectric Films zinc oxide and aluminum nitride, are well-suited to sputtering.



Sputtering Vacuum Deposition Process

Thin Film Deposition, CVD:

(2) Chemical Vapor Deposition (CVD):

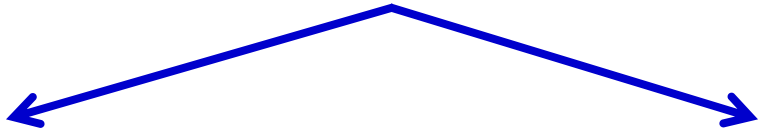
- A chemical reaction occurs on the surface of the wafer, resulting in deposition of a thin film on the wafer.
- A wide variety of materials can be deposited by CVD methods with great conformality.
- CVD process takes place in a special chamber or reactors.
- **Atmospheric Pressure** CVD (APCVD) results in high deposition rate. It is used mainly to deposit thick dielectrics like silicon nitride. On the other hand, the deposited material contains contamination.
- **Low Pressure** CVD (LPCVD) operates at 0.1 – 1 torr. It produces high quality **conformal films**. It is used to deposit silicon dioxide, polysilicon, tungsten and silicon nitride.
- **Plasma-Enhanced** CVD (PECVD) is a low temperature and low pressure process used to deposit silicon nitride.

Temperature range of 500-900 ˚C

TABLE 2.5
CVD Reactions

SiO_2	$SiH_4 + O_2 \rightarrow SiO_2 + H_2O$
	$SiH_4 + N_2O \rightarrow SiO_2 + NH_3 + H_2O$
	$SiO(CH_3)_4 + O_2 \rightarrow SiO_2 + CH_3 + O_2$
Si_3N_4	$SiH_4 + NH_3 \rightarrow Si_3N_4 + H_2$
	$SiH_4Cl_2 + NH_3 \rightarrow Si_3N_4 + HCl$
$Si^{(poly)}$	$SiH_4 \rightarrow Si + H_2$
W	$WF_6 + SiH_4 \rightarrow W + SiF_4 + H_2 + F_2$
TiN	$TCl_4 + NH_3 \rightarrow TiN + Cl_2 + H_2$

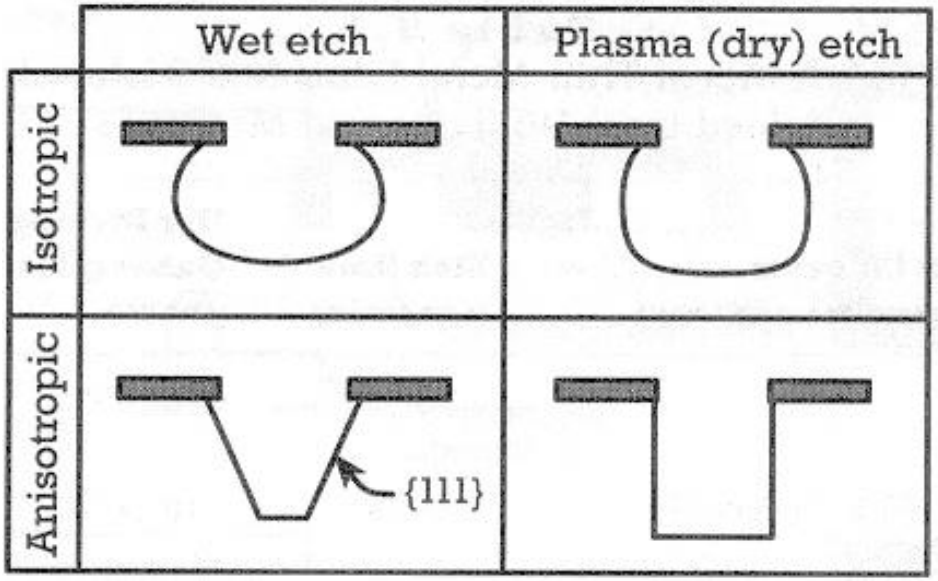
Fabrication Processes, Micromachining



Wafer level processes	Pattern transfer
Silicon wafers	Photoresist
Wafer cleaning	Photolithography
Oxidation of silicon	Mask polarity
Doping	
Thin film deposition	
Etching	
Electrodeposition (Elctroplating)	

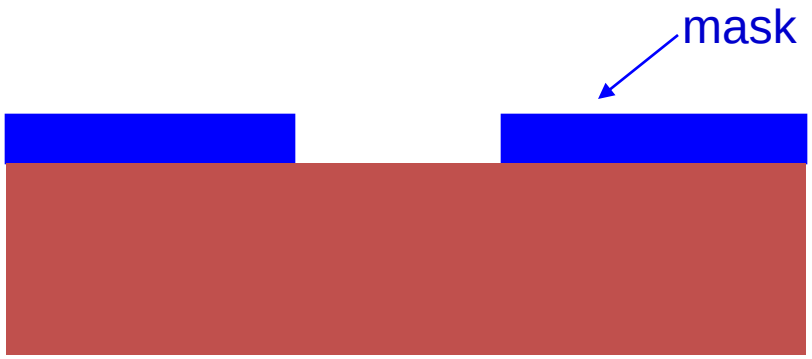
Etching

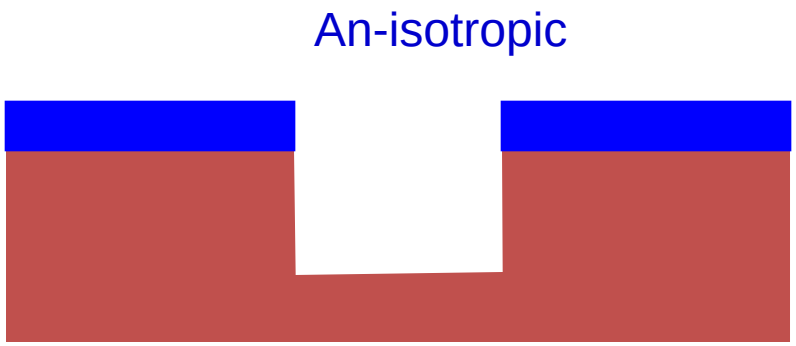
- Patterned wafers usually require etching. This may be the etching of thin films or in the silicon itself to form 3D structures. Etching can be classified as **wet etching (chemical)** or **dry etching (plasma etching)**. Each process results in a defined shape of etch pit, depending upon the characteristics of the etching process.

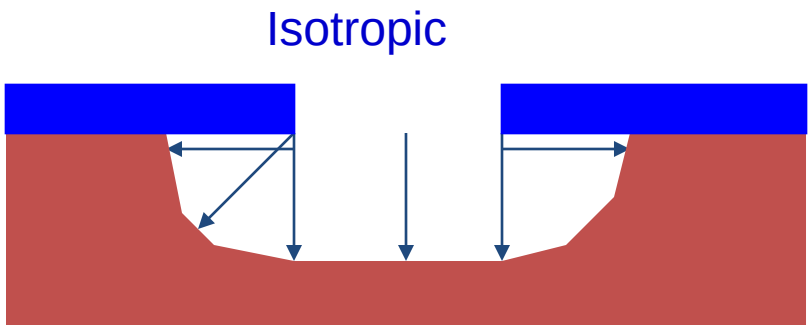


Etching issues, Anisotropy

- Isotropic etchants etch at the same rate in every direction.
- Anisotropic etchants etch at different rates in different directions.

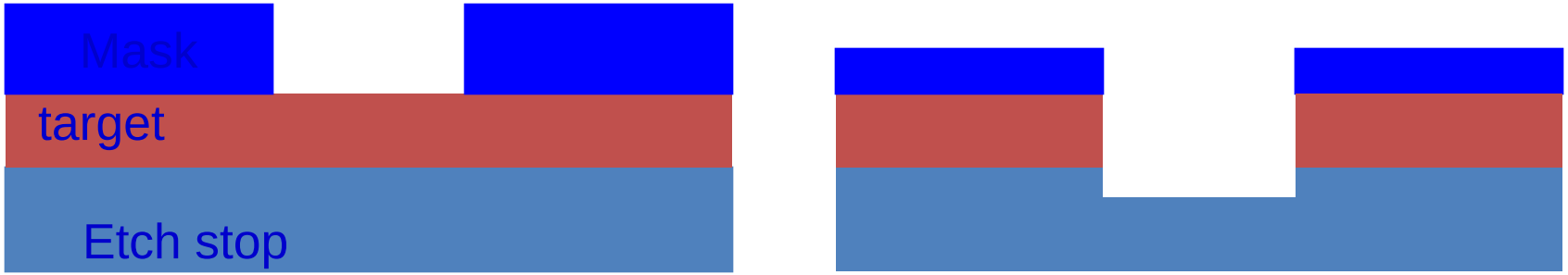




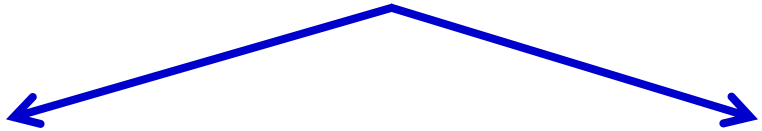


Etching issues, Selectivity

- Selectivity is the ratio of the etch rate of the target material being etched to the etch rate of other materials, mask and substrate.
- Chemical , wet, etching etches are generally more selective than plasma etches
- Selectivity to masking material and to etch-stop is important



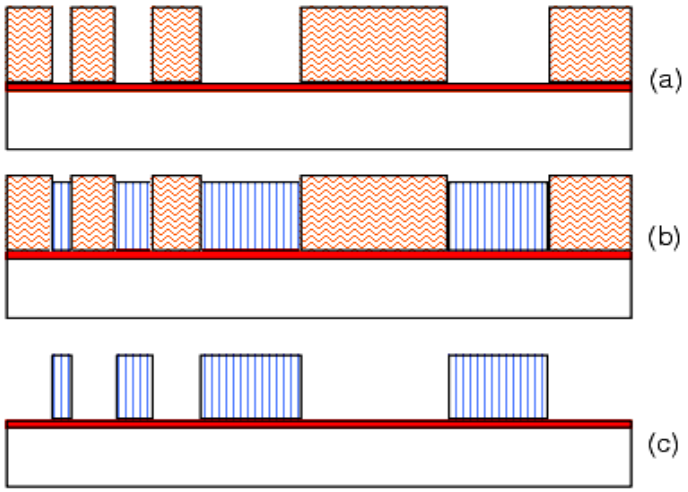
Fabrication Processes, Micromachining

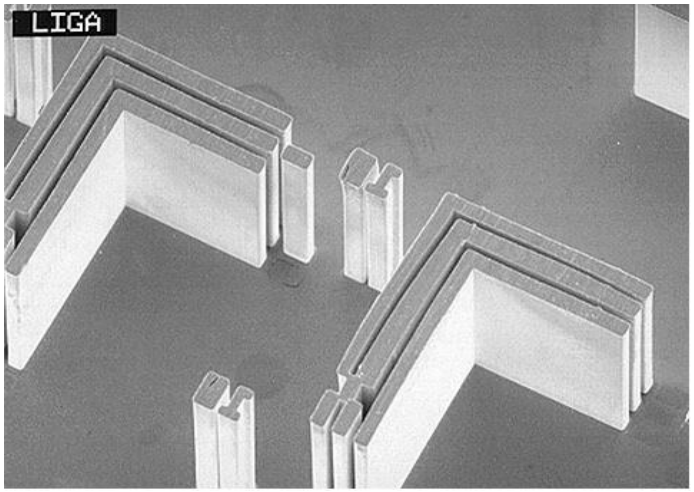


Wafer level processes	Pattern transfer
Silicon wafers	Photoresist
Wafer cleaning	Photolithography
Oxidation of silicon	Mask polarity
Doping	
Thin film deposition	
Etching	
Electrodeposition (Elctroplating)	

Electrodeposition

- Electrodeposition, or electroplating, is an electrochemical deposition process in which metal ions in solution are deposited onto a substrate with a metal seed layer.
- Metals that are well suited for plating are gold, copper, chromium, nickel, and magnetic iron-nickel alloys (permalloy).
- Most plating involves control with an applied electric current.
- Plating uniformity depends on maintaining a uniform current density everywhere the plating is done.
- Features of different areas, and regions at the corners of features, may plate at different rates.
- Plated metals often exhibit rougher surfaces than evaporated or sputtered films.





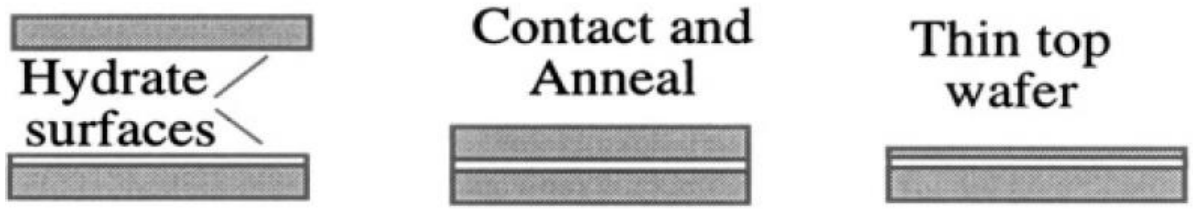
Wafer Bonding

Silicon Fusion Bonding:

- At room temperature, two highly polished flat silicon wafers brought into contact

will bond. The mechanism is believed to be hydrogen bonds between the surfaces.

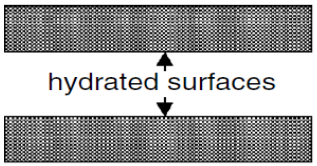
- The bond can be converted into a stronger bond at high temperature (~1000°C), annealing process.
- The main concern with this bonding technique is voids in the bonded wafer due to surface defects, residues, and particulate on the surface.
- Other silicon-based materials such as polycrystalline silicon (polysilicon), silicon dioxide, and silicon nitride can be similarly bonded.
- SOI (Silicon On Insulator) is fabricated using this method.

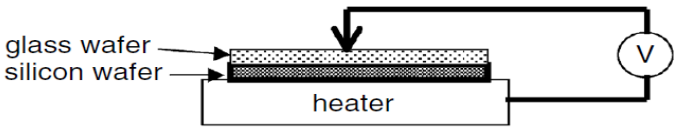


Wafer Bonding

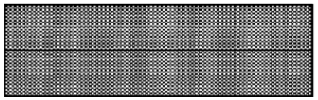
Anodic Bonding:

- Anodic bonding is an electrostatic bonding technique for **glass to silicon wafers** or silicon wafers with a thin silicon dioxide layer between the wafers.
- Anodic bonding utilizes a heated chuck with an electrode capable of applying a DC voltage of up to 1000 V.
- Pressure may be applied to facilitate the bonding process.
- Requires a temperature of 400 ºC with large electric field.

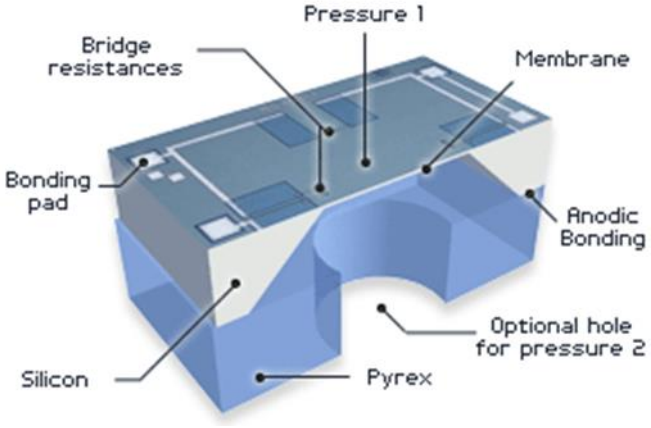




(a) Silicon wafers with hydrated surfaces.

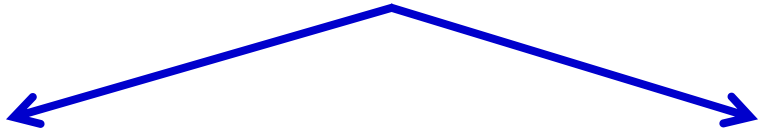


(b) Silicon wafers in contact and anneal.



MEMS-based pressure sensor

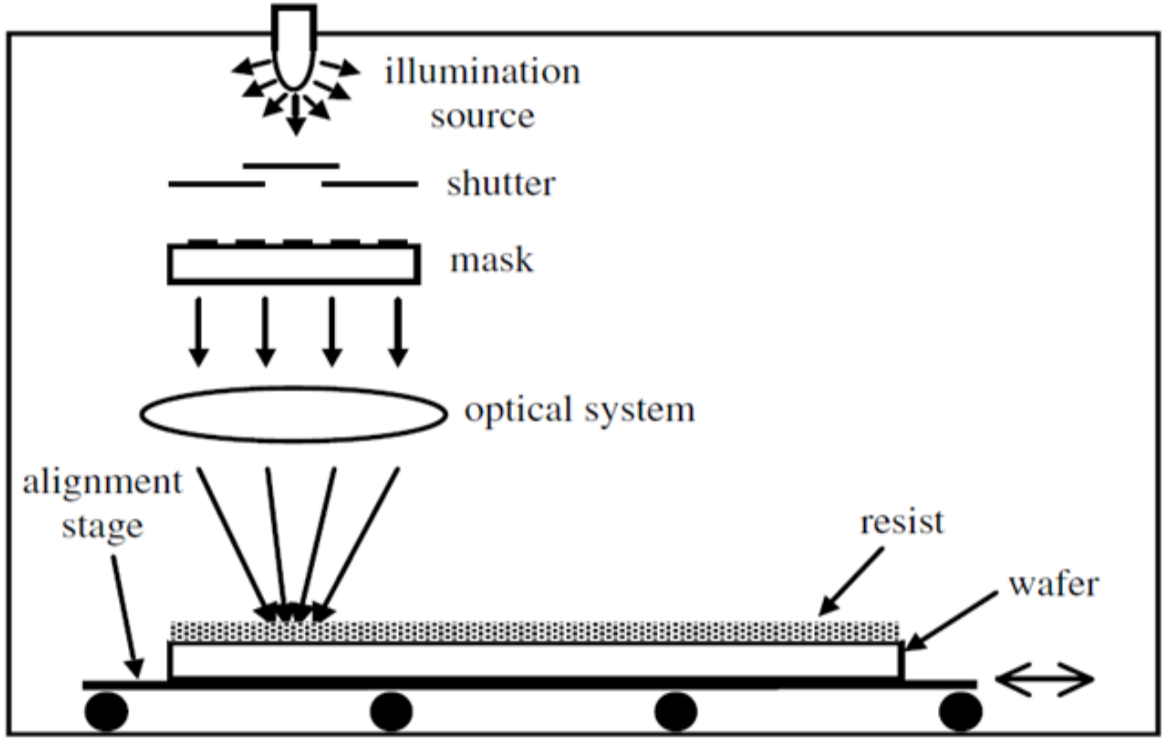
Fabrication Processes, Micromachining



Wafer level processes	Pattern transfer
Silicon wafers	Photolithography
Wafer cleaning	Photoresist
Oxidation of silicon	Mask polarity
Doping	
Thin film deposition	
Etching	
Electrodeposition (Elctroplating)	

Pattern Transfer, Lithography

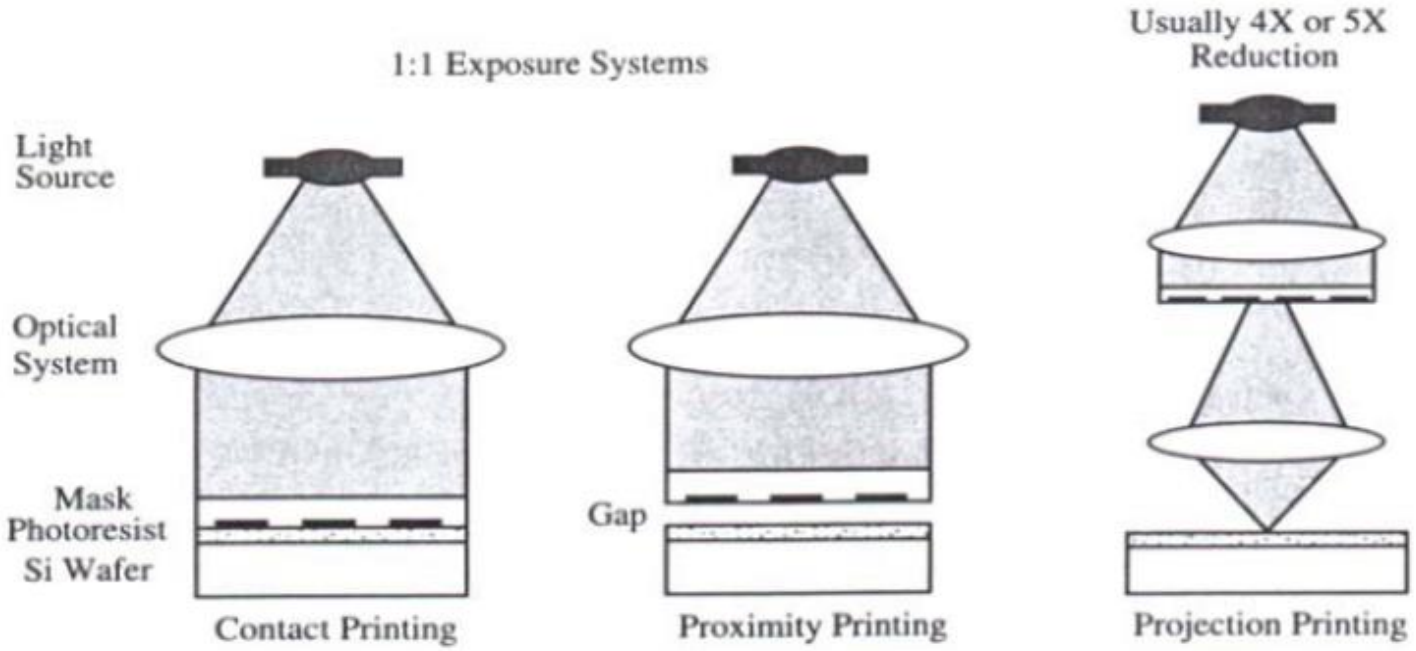
- Lithography is a key batch fabrication process in both IC and MEMS fabrication.
- Lithography is the most critical process in IC and MEMS processes.
- The photolithographic system contains:
  - Illumination source
  - Shutter
  - Mask with/without an optical system
  - Photosensitive layer (photoresist)
  - Wafer alignment/support system



Projection (step and repeat) lithography

Pattern Transfer, Lithography

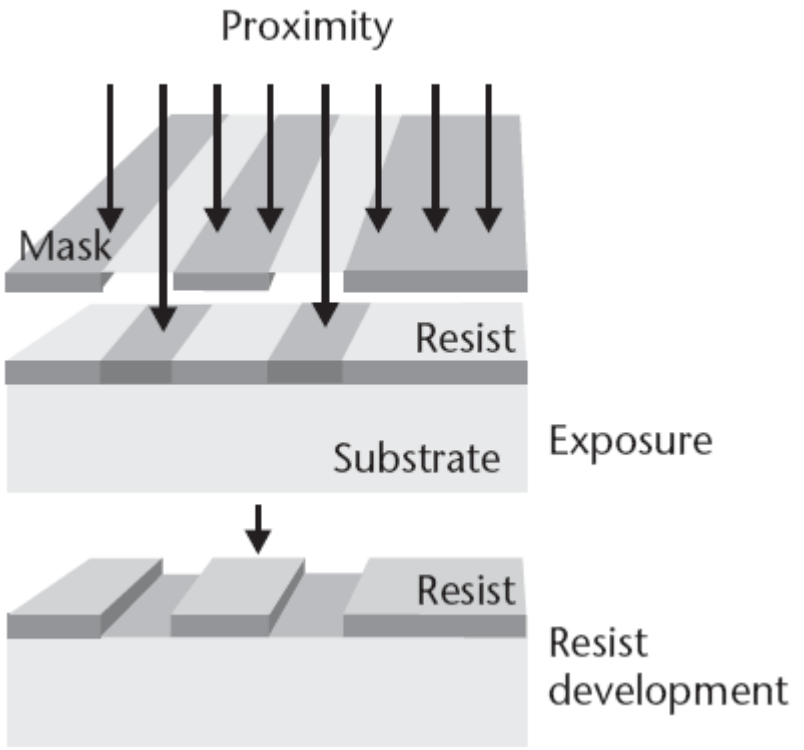
- There are 3 basic lithographic methods:
  - Contact lithography
  - Proximity lithography
  - Projection (step and repeat) lithography



Pattern Transfer, Lithography

❑ Contact/Proximity lithography:

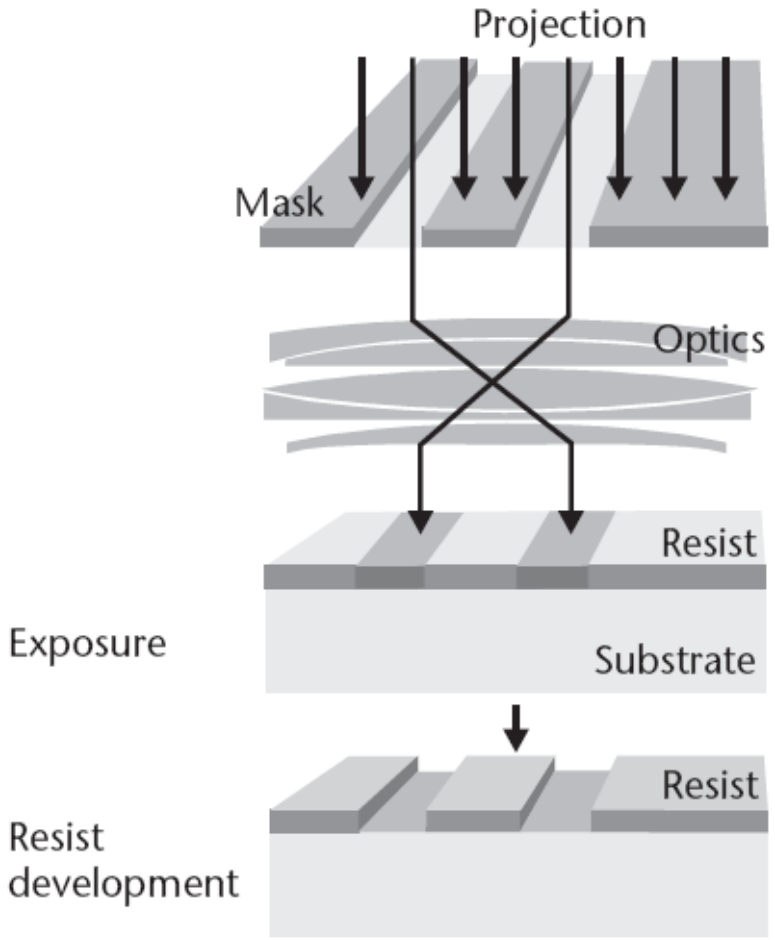
- The mask is held in contact or close (few microns) of the photoresist surface.
- The mask and the substrate have same size.
- Features on the mask have same size as on the substrate (scale of 1x1)
- Mask may damage because of the contact.
- Least expensive photolithography system.
- Lowest resolution (~1-2 microns).
- Limited production applications.



Pattern Transfer, Lithography

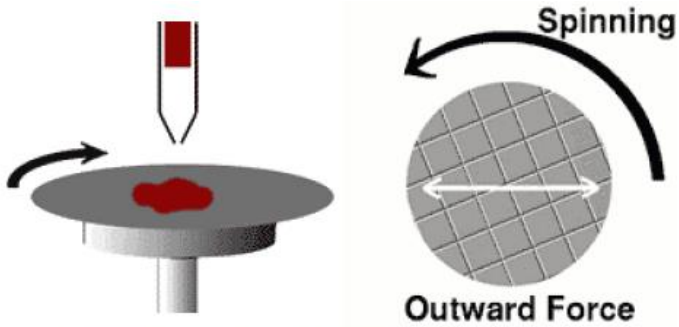
❑ Projection lithography:

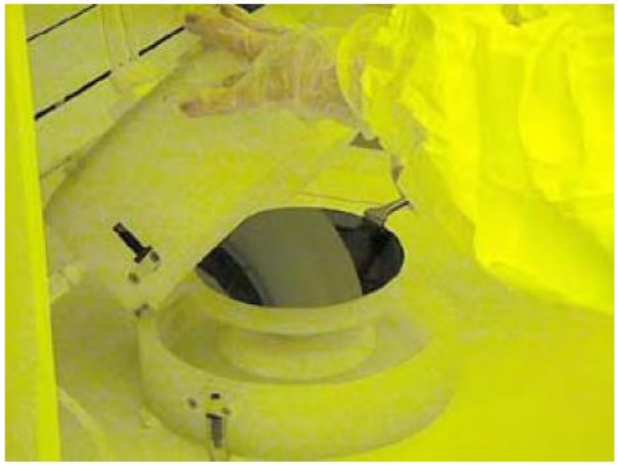
- Mask and wafer are separated.
- Optical reduction 2x-10x is placed between the mask and the wafer.
- High resolution (< 1 micron).
- Automated moving stages.
- Complicated system.
- Most expensive.
- High volume production applications.

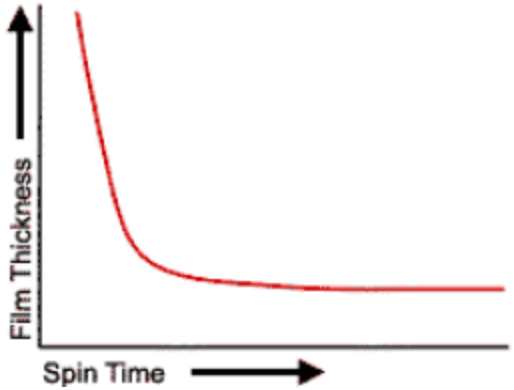


Pattern Transfer, Photoresist

- Photoresist is a photosensitive material (polymer) that is spun on the wafer surface.
- Photoresist is an organic compound that dissolves or hardens when it is exposed to UV (Ultraviolet) light (wavelength ~ 380 - 400 nm).
- Thickness of photoresist layer depends on:
  - Viscosity
  - Spinning time
  - Spinning speed

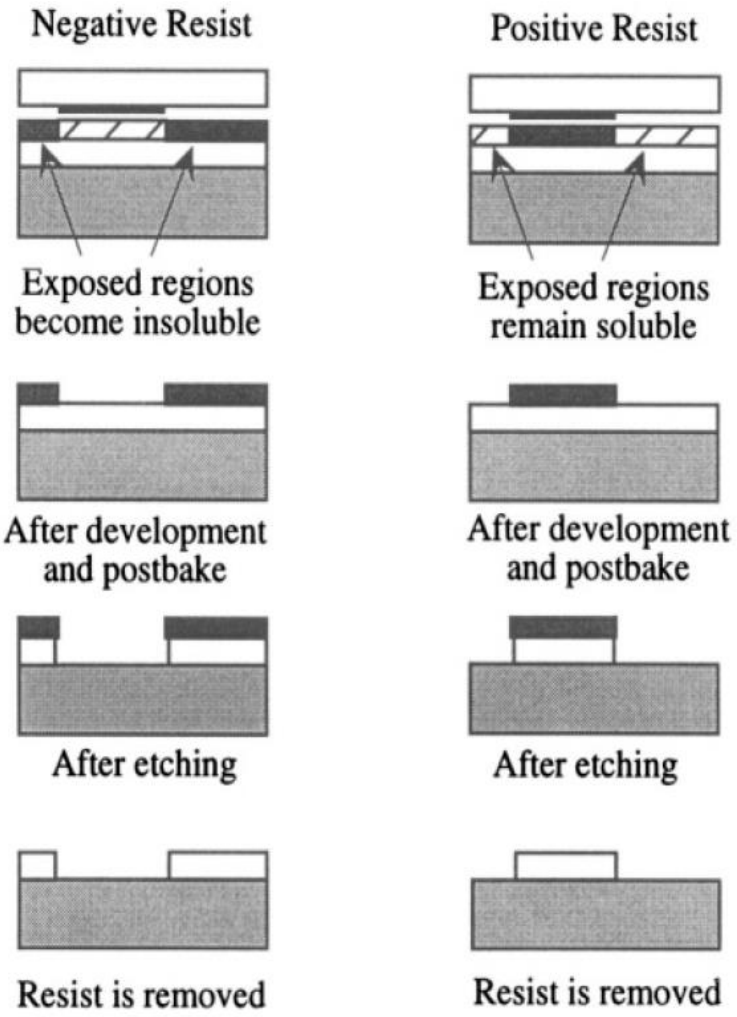






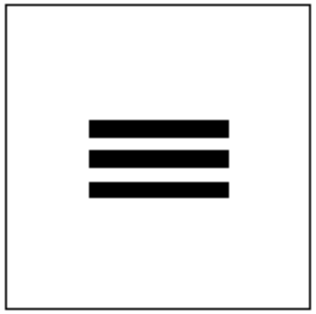
Pattern Transfer, Photoresist

- Photoresist is either a positive or negative polarity:
- Positive photoresist: The region of photoresist that has been exposed to the UV light will dissolve during the developing process and be removed.
- Negative photoresist: The region of photoresist that has **not** been exposed to the UV light will dissolve during the developing process and be removed. in other words, the region that has been exposed to the light will harden and will not be removed during the developing process (opposite of positive photoresist)
- Positive photoresist has better resolution than negative photoresist ➔ more frequently used.
- After removal, remaining PR is the physical mask for subsequent process, etching, deposition.

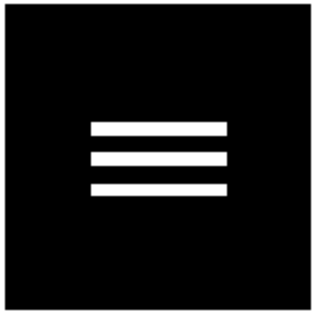


Pattern Transfer, Mask polarity

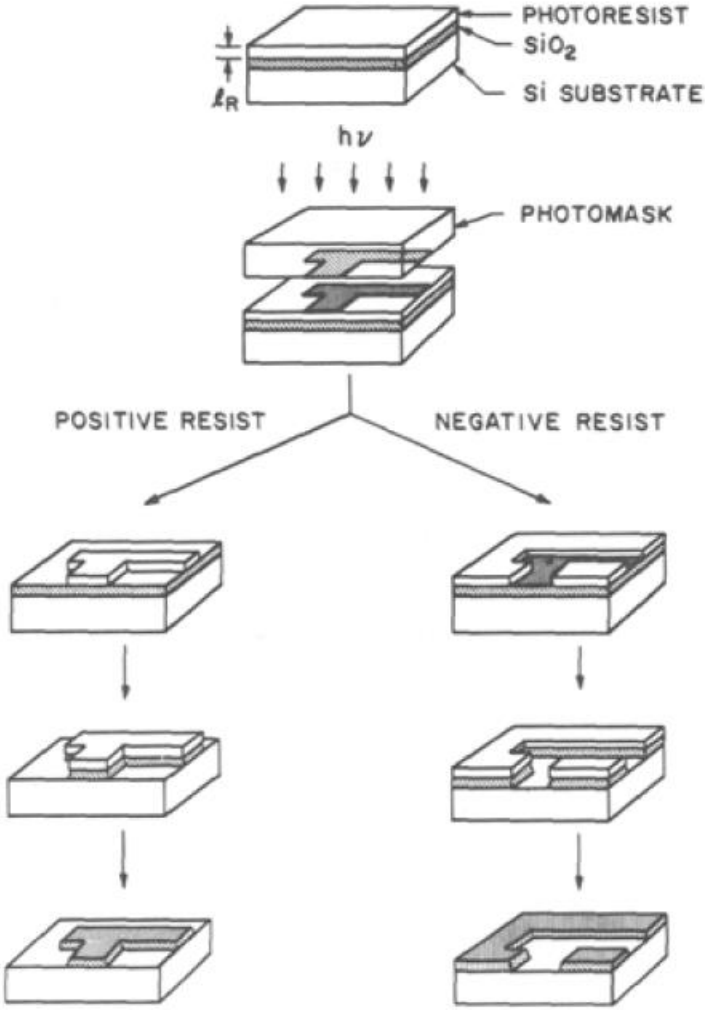
- Mask is either bright (light)-field or dark-field.
- Mask is generated from a CAD file.
- Patterned chrome on glass strip.



light-field



dark-field

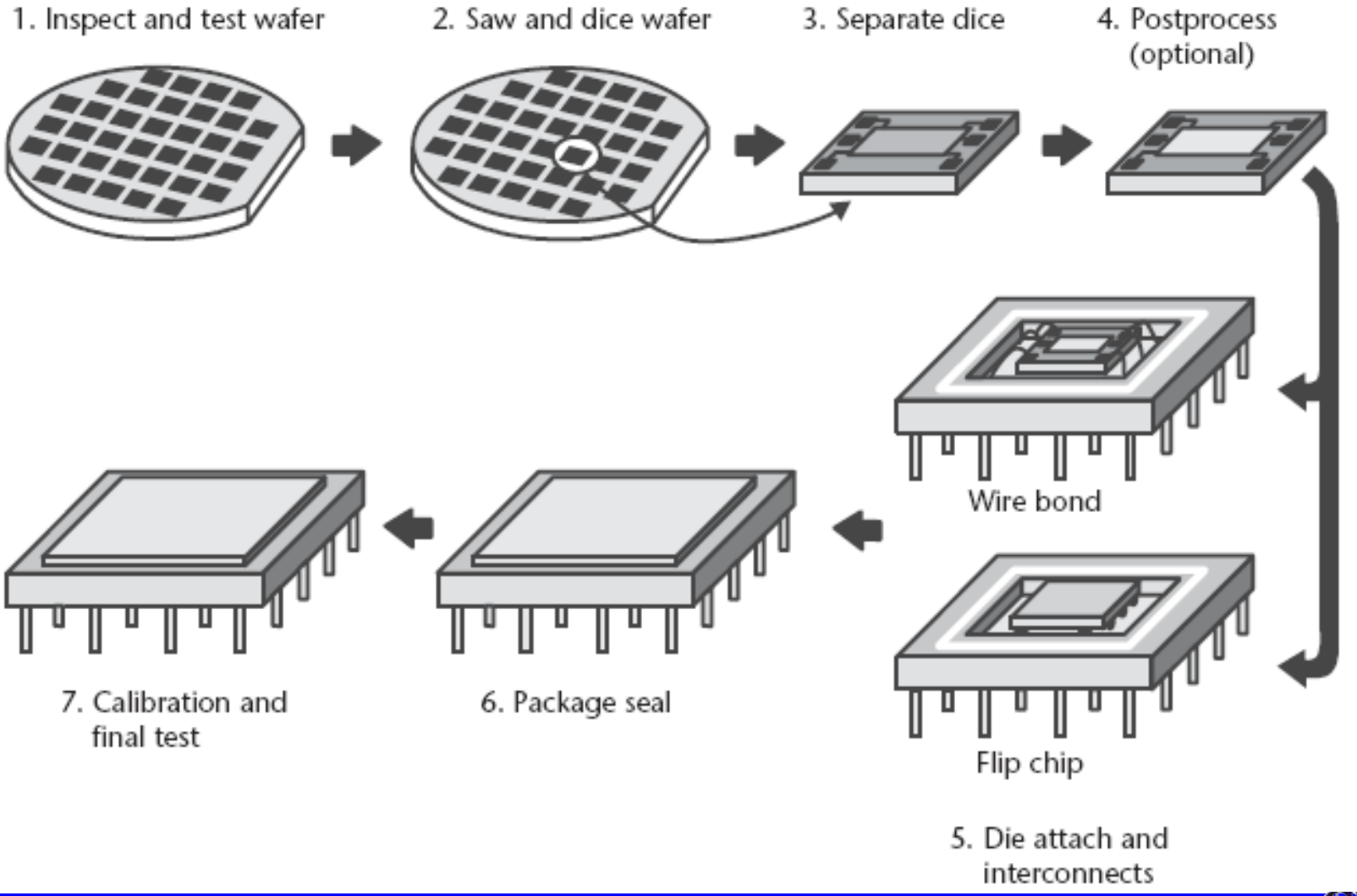


Back-End Processes

Packaging and Reliability Considerations

- Packaging is the process of encapsulating components inside protective packages.
- It transforms a micromachined structure into a useful assembly that can safely and reliably interact with the surrounding.
- Functions of a package are:
  - Protection of MEMS structure.
  - Providing electrical access.
  - Allows interaction with external environment.
- MEMS packaging is not standard, it differs from one application to another.
- MEMS packaging is more expensive than the component itself.

Back-End Process Flow



Wafer Dicing Considerations

- Dicing is carried out by a mechanical saw with diamond blade approximately 50 µm wide
- This subjects MEMS structures to a lot of heat, that is why it is continuously flushed with water
- This harsh environment including stress, water flushing and flying debris my damage MEMS structure specially if already released
- Release may preferably be done after dicing to avoid MEMS damage
- Alternatively, Laser dicing may be used

Hermetic Packaging

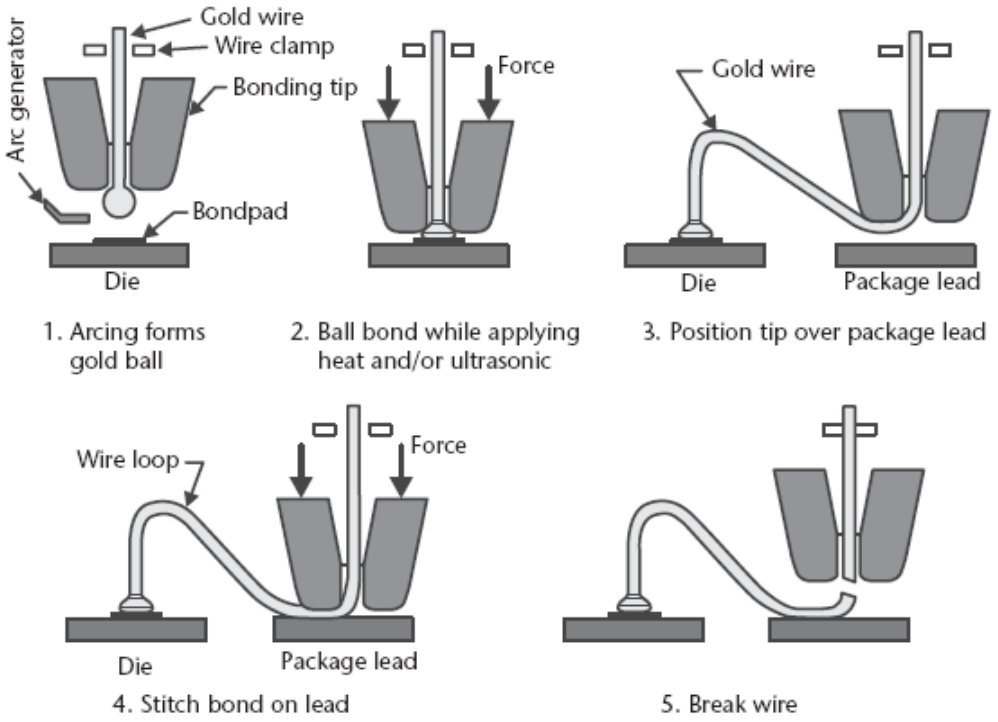
- Hermetic packages are air tight and prevent diffusion of small molecules thus perfectly isolating MEMS structures from the surrounding ambient
- Hermetic packages can be made of ceramics, Silicon, glass
- Plastics and organic compounds allows diffusion of moisture
- Hermetic packages are expensive but enhance reliability and life time

Die Attach Material Considerations

- Die attach material has to address thermal management, electrical isolation and mechanical stress considerations
  - Die attach material has to provide electrical isolation or conduction depending on the specific case
  - It plays a role in thermal management and in providing good thermal expansion matching between package and die
- Die attach materials may be:
  - Metal alloys / solders
  - Organic adhesives, epoxies, silicones

Wire Bonding

- *Thermosonic* gold bonding simultaneously combines the application of heat, pressure, and ultrasonic energy to the bond area.
- Ultrasound causes the wire to vibrate, producing localized frictional heating to aid in the bonding process.
- Typically, the gold wire forms a *ball bond* to the aluminum bond pad on the die and a *stitch bond* to the package lead.
- The stitch bond is a wedge-like connection as the wire is pressed into contact with the package lead (typically gold or silver plated). The temperature of the substrate is usually near 150ºC
- The use of ultrasonic energy may cause MEMS structures and oscillate and may cause consequent damage



Flip-Chip

- Flip-chip bonding, as its name implies, involves bonding the die, top face down, on a package substrate.
- Electrical contacts are made by means of plated solder bumps between bond pads on the die and metal pads on the package substrate.
- The attachment is intimate with a relatively small spacing (50 to 200 μm) between the die and the package substrate.
- Unlike wire bonding which requires the bond pads to be positioned on the periphery of the die to avoid crossing wires, flip chip allows the placement of bond pads over the entire die
- Additionally, the effective inductance of each interconnect is minuscule because of the short height of the solder bump. The inductance of a single solder bump is less than 0.05 nH, compared to 1 nH for a 125 μm long and 25 μm diameter wire
- Alternatively, Flip Chip bonding can be used to bond two dies together