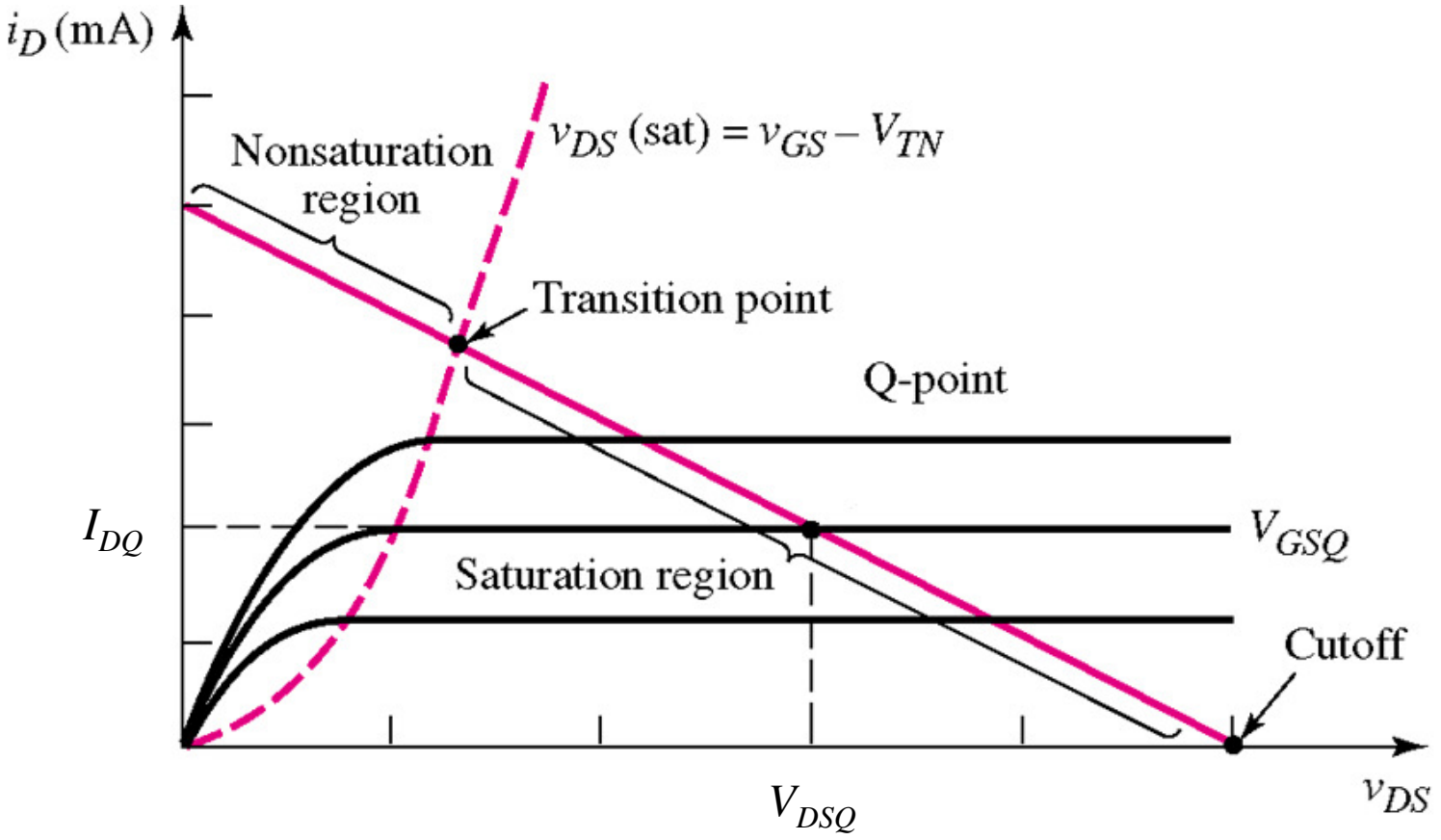
Faculty of Engineering

ECE 335: Electronic Circuits

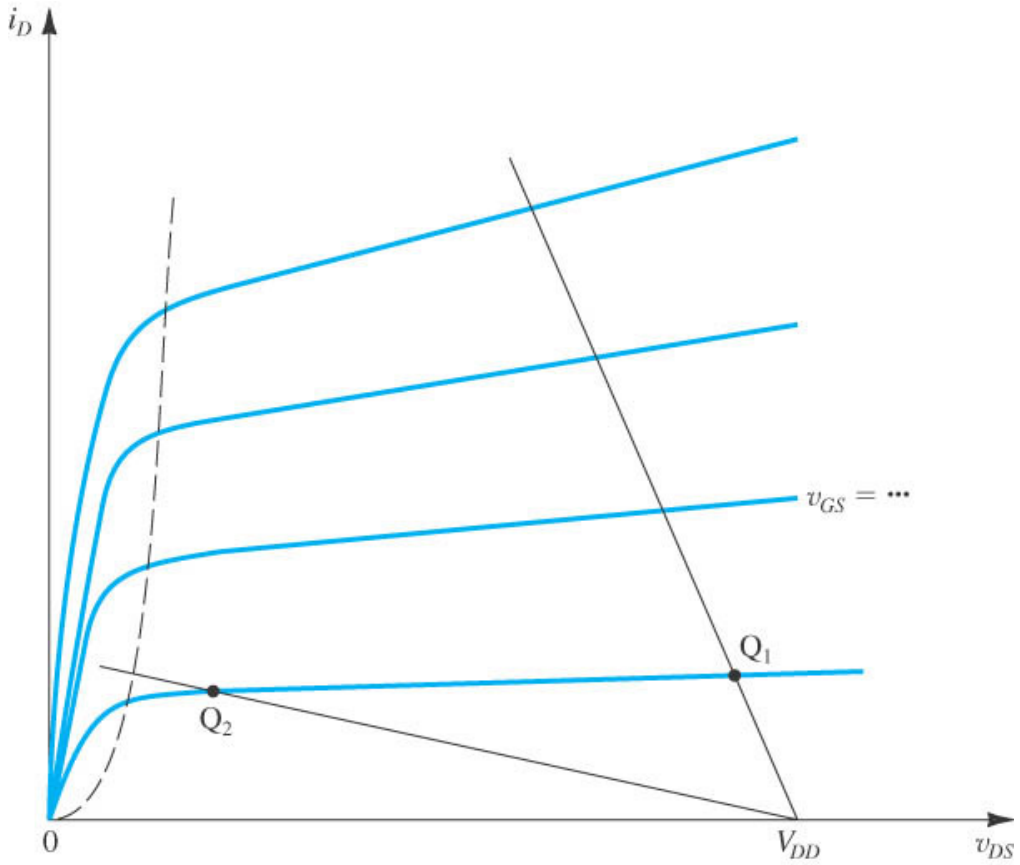
Lecture 8:
MOSFET Small Signal Model

Graphical Analysis, Load Lines



Common-source transistor characteristic

Graphical Analysis, Load Lines



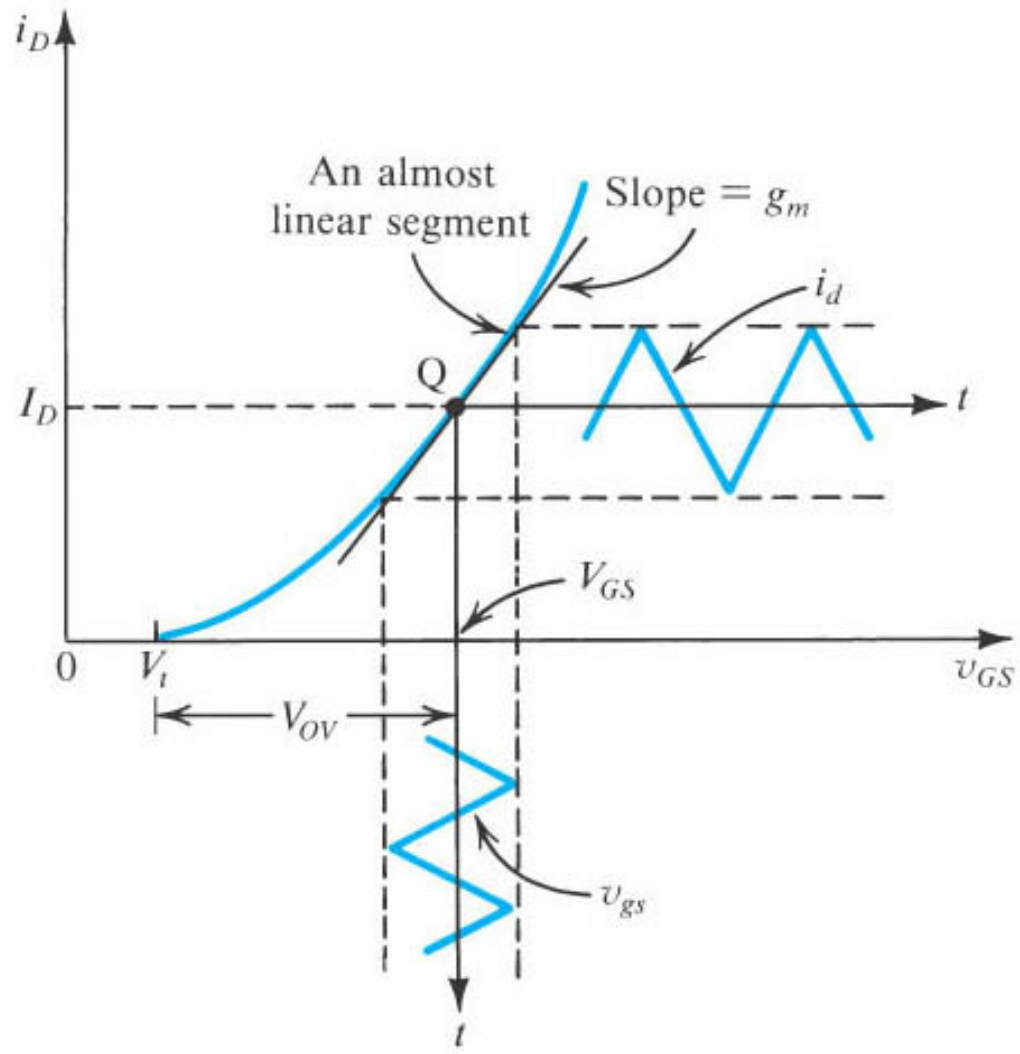
Two load lines and corresponding bias points. Bias point Q_1 does not leave sufficient room for positive signal swing at the drain (too close to V_{DD}). Bias point Q_2 is too close to the boundary of the triode region and might not allow for sufficient negative signal swing.

MOSFET Parameters

- Transconductance, g_m

$$g_m = \frac{i_d}{v_{gs}} = \frac{\partial I_D}{\partial V_{GS}}$$

$$= \frac{2I_D}{V_{GS} - V_{th}}$$



Example: Transconductance

Exercise

The transistor has K_P=50μA/V², V_t=2V, L=10μm, and W=400μm

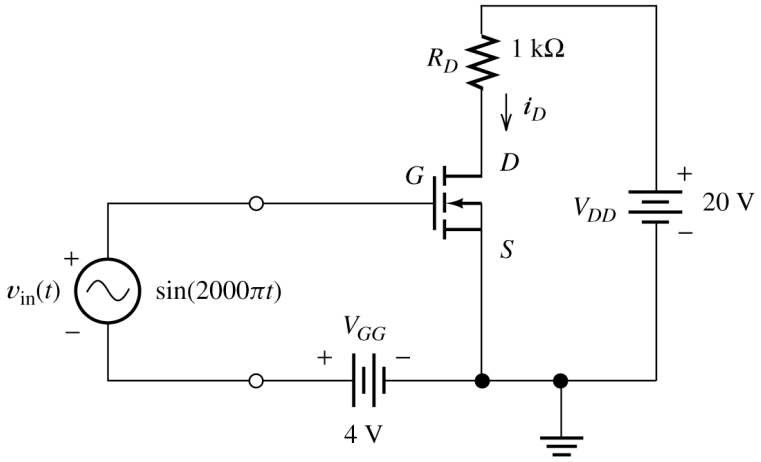
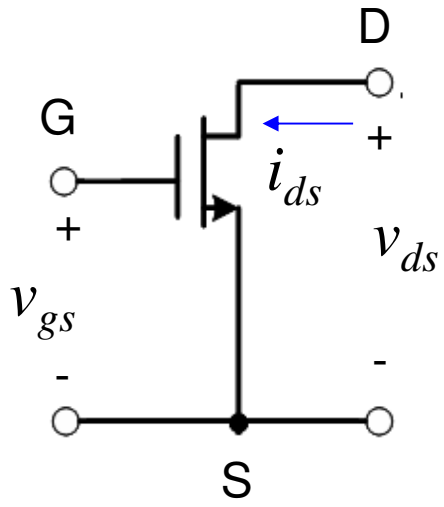


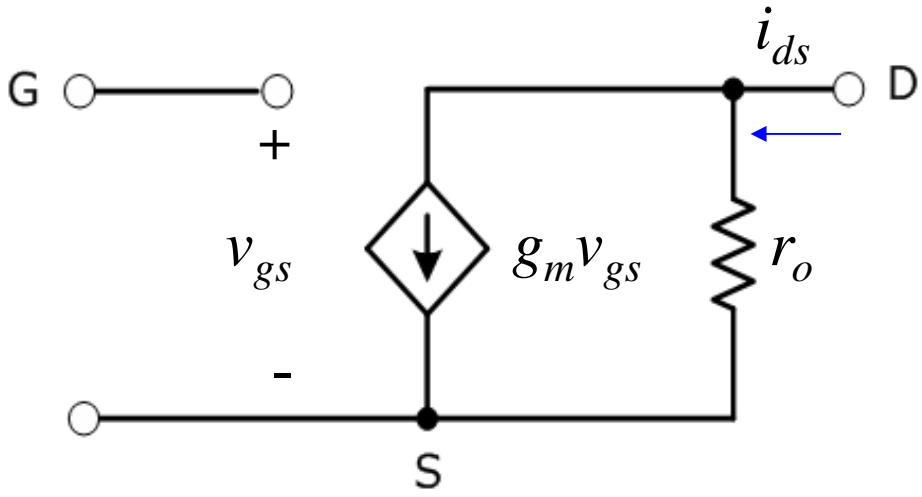
Figure 12.10 Simple NMOS amplifier circuit.

$$I_D = \frac{K_P}{2}\left(\frac{W}{L}\right)(V_{GS} - V_{th})^2 = 4mA/V^2$$

$$g_m = \frac{2I_D}{V_{GS} - V_{th}} = \frac{2\times 4}{4-2} = 4mS$$

MOSFET Small-Signal Equivalent Circuit





Common source NMOS with small signal parameters

Simplified small signal equivalent circuit for NMOS

Small-signal output resistance

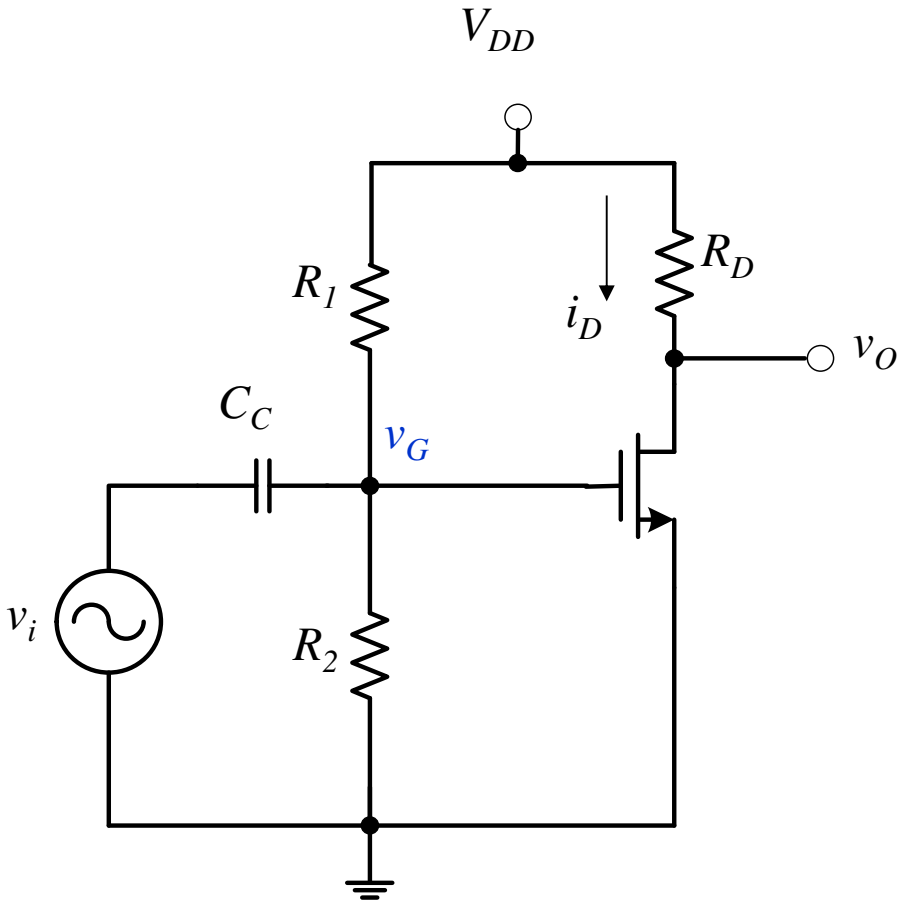
$$r_o = \frac{V_A}{I_{DQ}} = \left(\lambda I_{DQ}\right)^{-1}$$

where

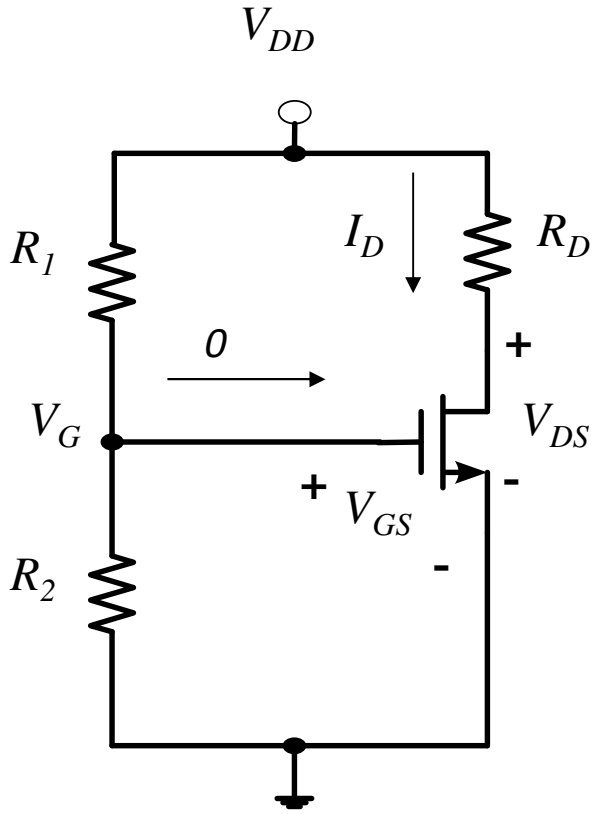
$$\lambda = \frac{1}{V_A}$$

DC Analysis

– Saturation Region

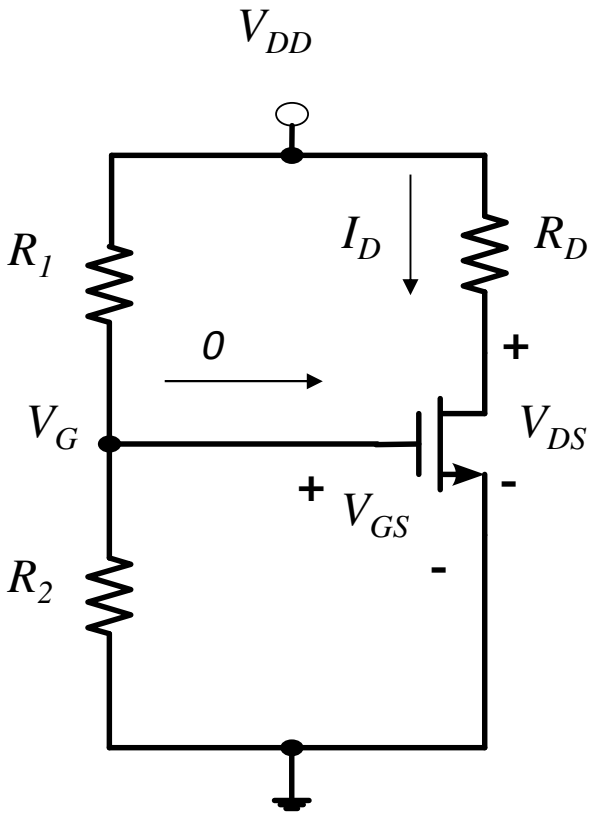


Voltage-divider circuit for MOSFET



DC equivalent circuit

DC Analysis
– Saturation Region



DC equivalent circuit

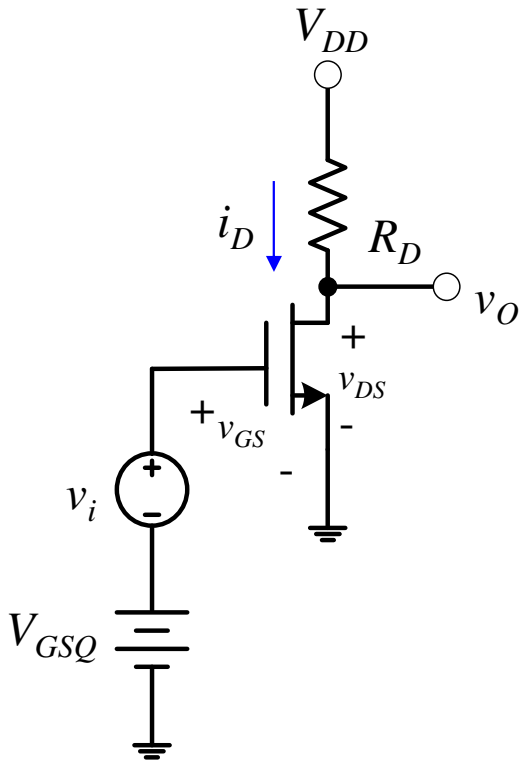
$$V_G = V_{GS} = \left(\frac{R_2}{R_1 + R_2} \right) V_{DD}$$

$$I_D = K(V_{GS} - V_{TN})^2$$

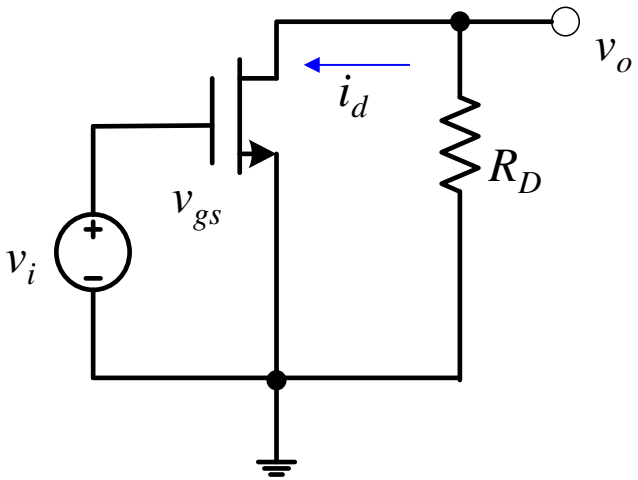
$$V_{DS} = V_{DD} - I_D R_D$$

$$V_{DS}(\text{sat}) = V_{GS} - V_{TN}$$

AC Analysis



NMOS common source circuit with time-varying signal source in series with gate DC source

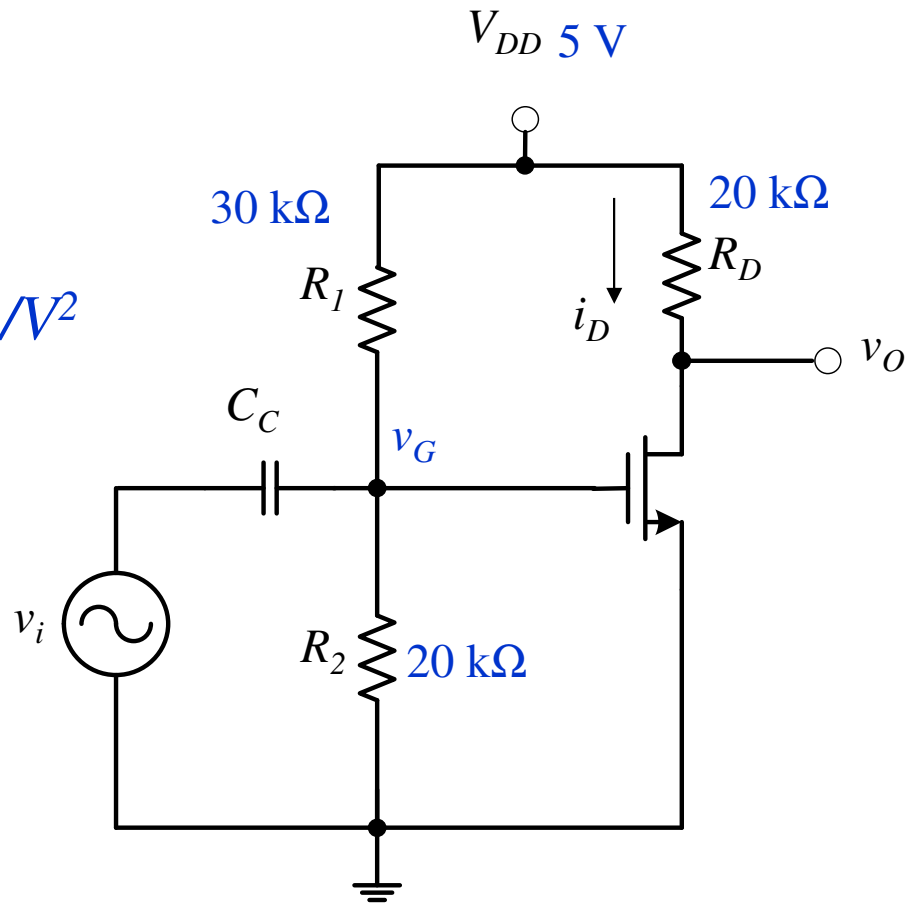


AC equivalent circuit

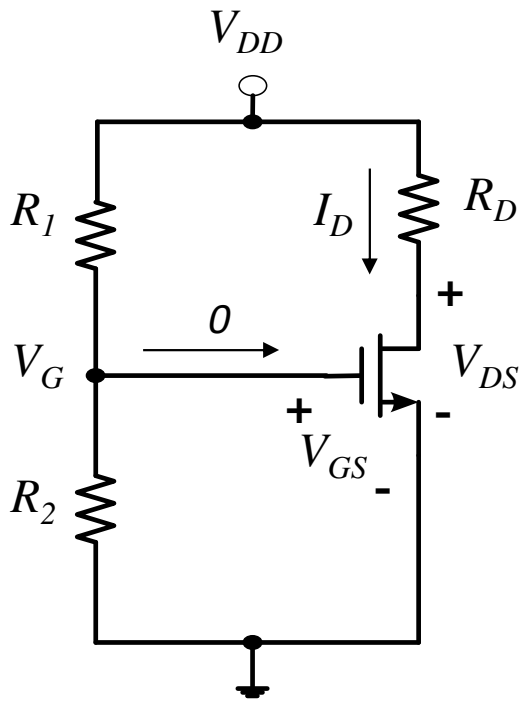
Example

$V_{TN} = 1\ V$

$K_n W/L = 0.2\ mA/V^2$



DC equivalent circuit



$$V_G = V_{GS} = \left(\frac{R_2}{R_1 + R_2}\right) V_{DD} = \left(\frac{20}{20+30}\right) 5 = 2V$$

$$I_D = \frac{K_n}{2}\frac{W}{L}(V_{GS} - V_{TN})^2 = (0.1)(2-1)^2 = 0.1\,mA$$

$$V_{DS} = V_{DD} - I_D R_D = 5 - (0.1)(20) = 3V$$

The transistor is biased in the saturation region because $V_{DS} > V_{DS(sat)}$;

since $V_{DS(sat)} = V_{GS} - V_{TN} = 2 - 1 = 1$ V