Faculty of Engineering

ECE 334: Electronic Circuits

Lecture 10:
Digital CMOS Circuits

CMOS Technology

- Complementary MOS, or CMOS, needs both PMOS and NMOS FET devices for their logic gates to be realized
- The concept of CMOS was introduced in 1963 by Frank Wanlass and Chi-Tang Sah of Fairchild
  - did not become common until the 1980's as NMOS microprocessors were dissipating as much as 50W and alternative design techniques were needed
- CMOS still dominates digital IC design today

Properties of NMOS and CMOS Logic Gates

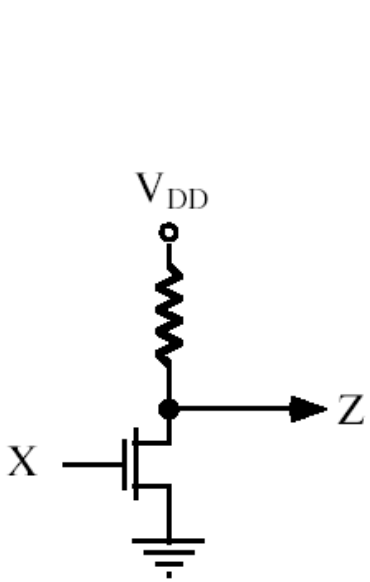
- No current flows through the gate unless the input signal is changing
  - High input impedance
  - High fan-out
- Sandwich structure of MOS transistor creates capacitor between the gate and substrate
  - High input capacitance
  - Slows transition time
  - Limits fan-out or switching speed
- NMOS dissipates power in low output state
- CMOS gate only dissipates power when it is changing state
  - The faster a CMOS gate switches the more power it dissipates, so there is a tradeoff between speed and power

Why CMOS is Better

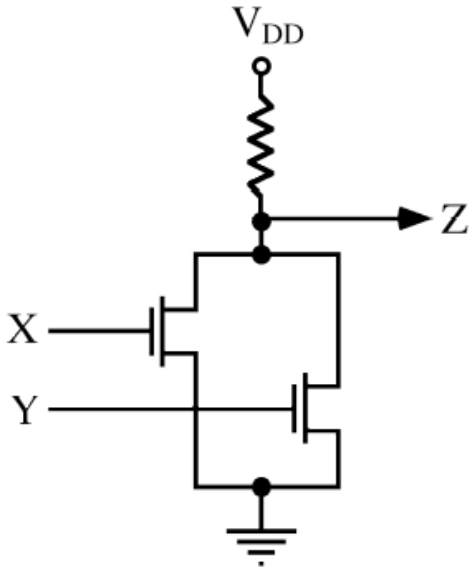
- Low DC Power Consumption
- Abrupt & well defined Voltage transfer Characteristic
- Noise Immunity due to Low impedance between logic levels and Supply/Gnd.
- Symmetry between T_{fall} & T_{rise}
- High Density: Si real estate → Yield → Cost
- Highly Integrated → Active & High input Impedance → Composition equality
- No real trade off between the above

NMOS Logic

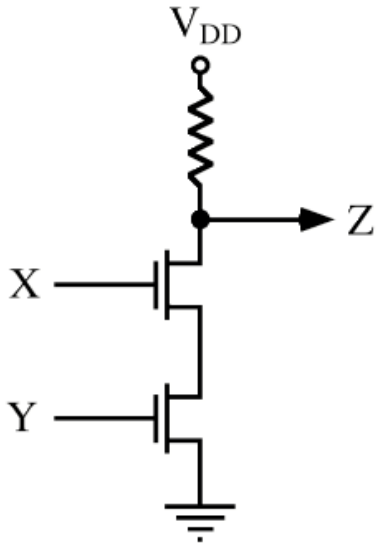
- Negative charge carriers (electrons)
- Positive biasing voltage at gate



NMOS Inverter



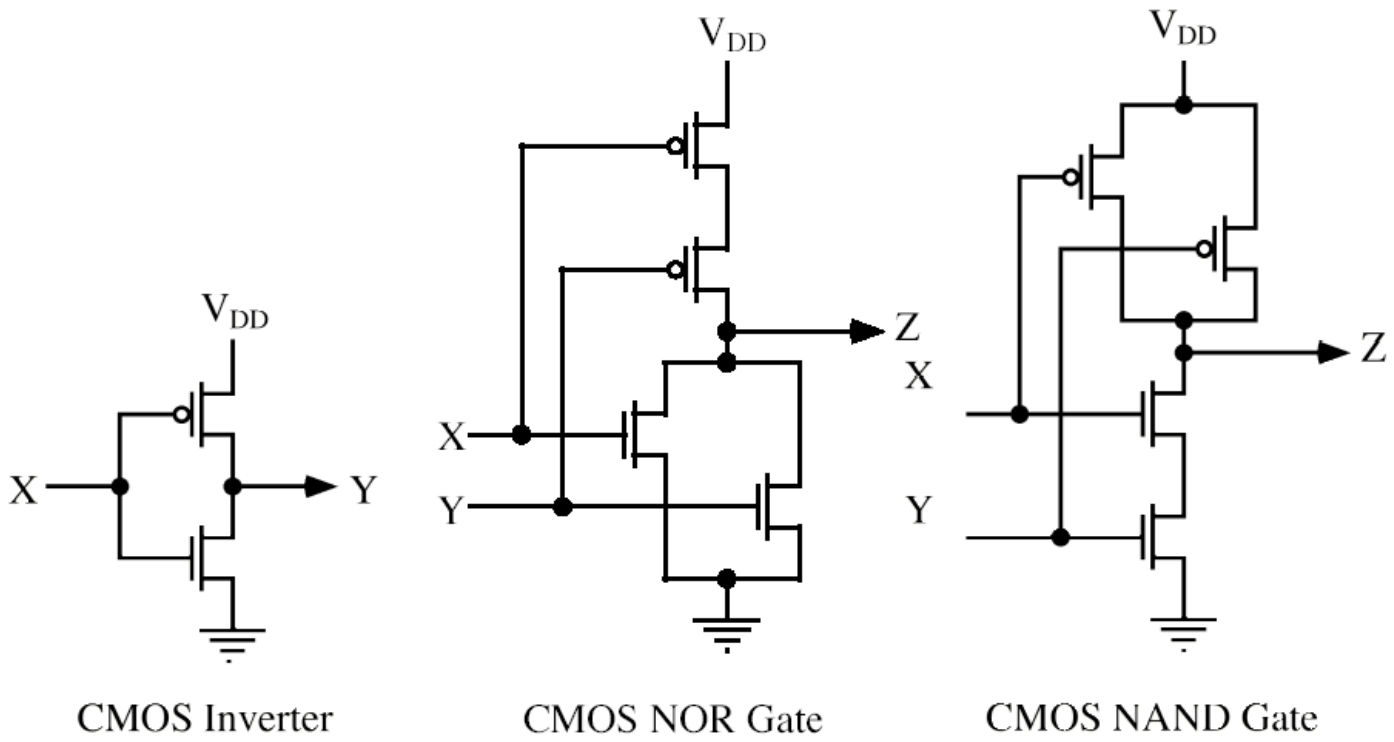
NMOS NOR Gate



NMOS NAND Gate

CMOS Logic

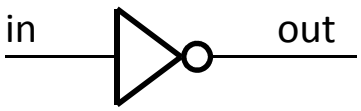
- Transistors come in complementary pairs



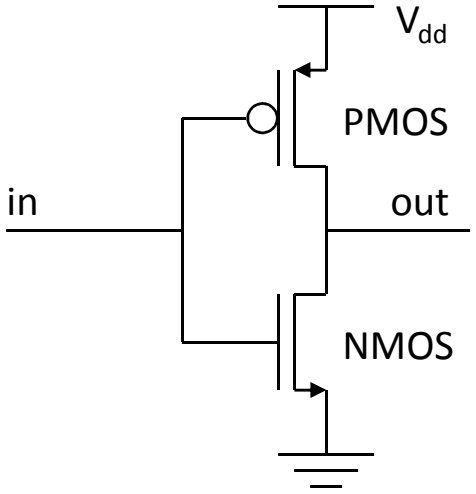
CMOS Inverter CMOS NOR Gate CMOS NAND Gate

CMOS Inverter

- CMOS gates are built around the technology of the basic CMOS inverter:



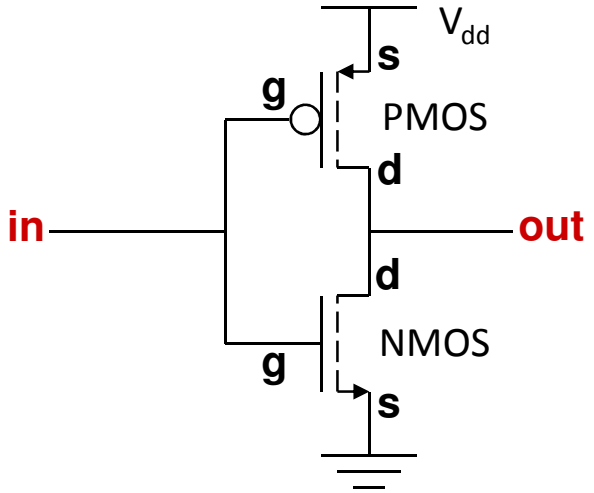
Symbol



Circuit

Basic CMOS Logic Technology

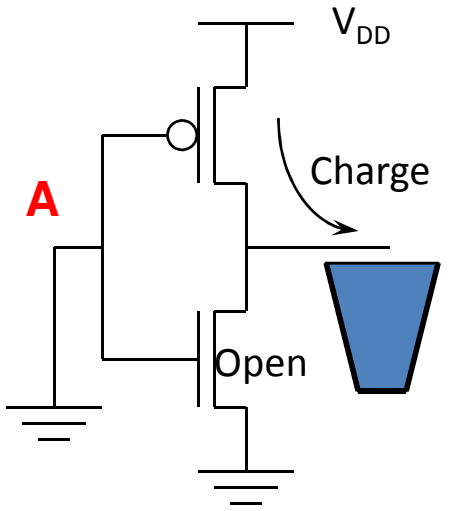
- Based on the fundamental inverter circuit at right
- Transistors (two) are enhancement mode MOSFETs
  - N-Channel with its source grounded
  - P-Channel with its source connected to +V
- Input: gates connected together
- Output: drains connected



CMOS Inverter - Operation

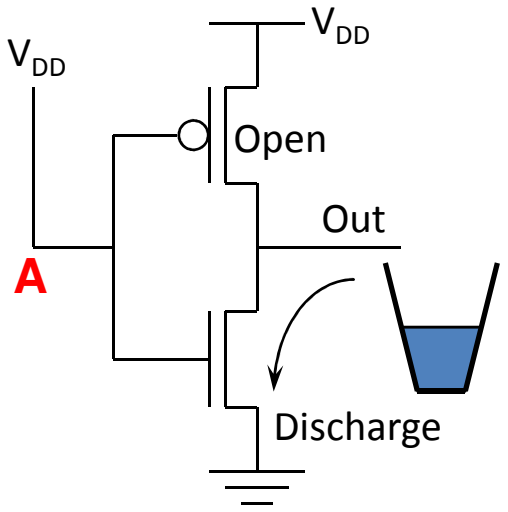
When input **A** is grounded (logic 0), the N-Channel MOSFET is unbiased, and therefore has no channel enhanced within itself. It is an open circuit, and therefore leaves the output line disconnected from ground.

At the same time, the P-Channel MOSFET is forward biased, so it has a channel enhanced within itself, connecting the output line to the $+V_{DD}$ supply. This pulls the output up to $+V_{DD}$ (logic 1).



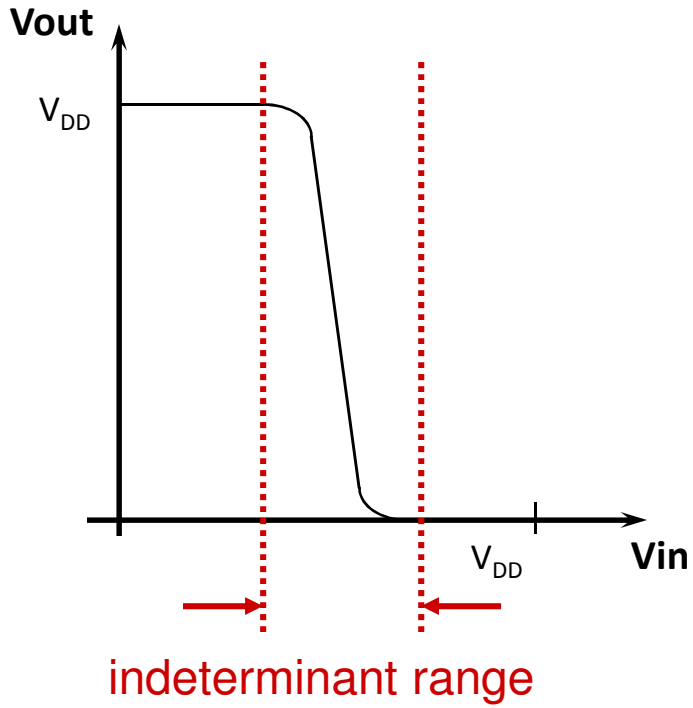
CMOS Inverter - Operation

When input **A** is at $+V_{DD}$ (logic 1), the P-channel MOSFET is off and the N-channel MOSFET is on, thus pulling the output down to ground (logic 0). Thus, this circuit correctly performs logic inversion, and at the same time provides active pull-up and pull-down, according to the output state.

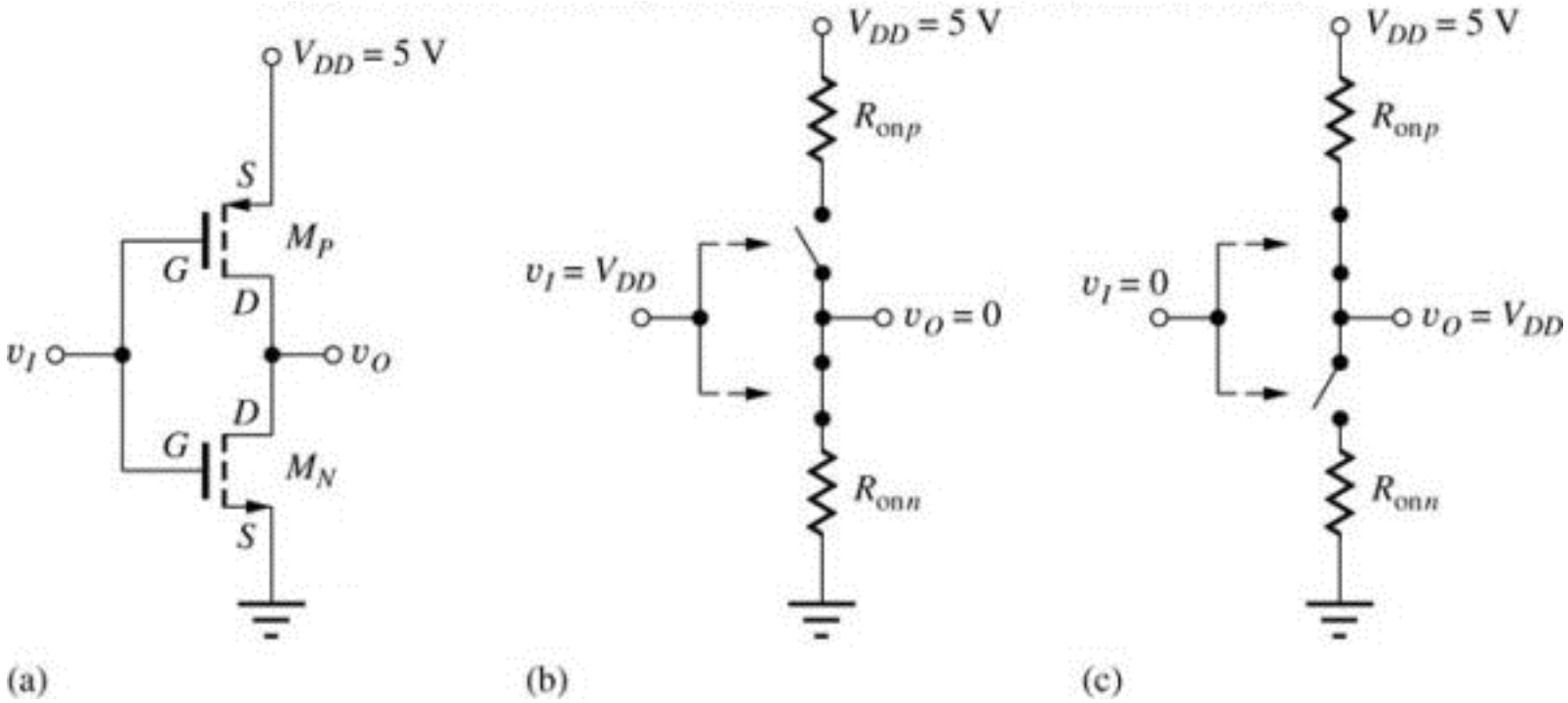


CMOS Inverter - Operation

Since the gate is essentially an open circuit it draws no current, and the output voltage will be equal to either ground or to the power supply voltage, depending on which transistor is conducting.

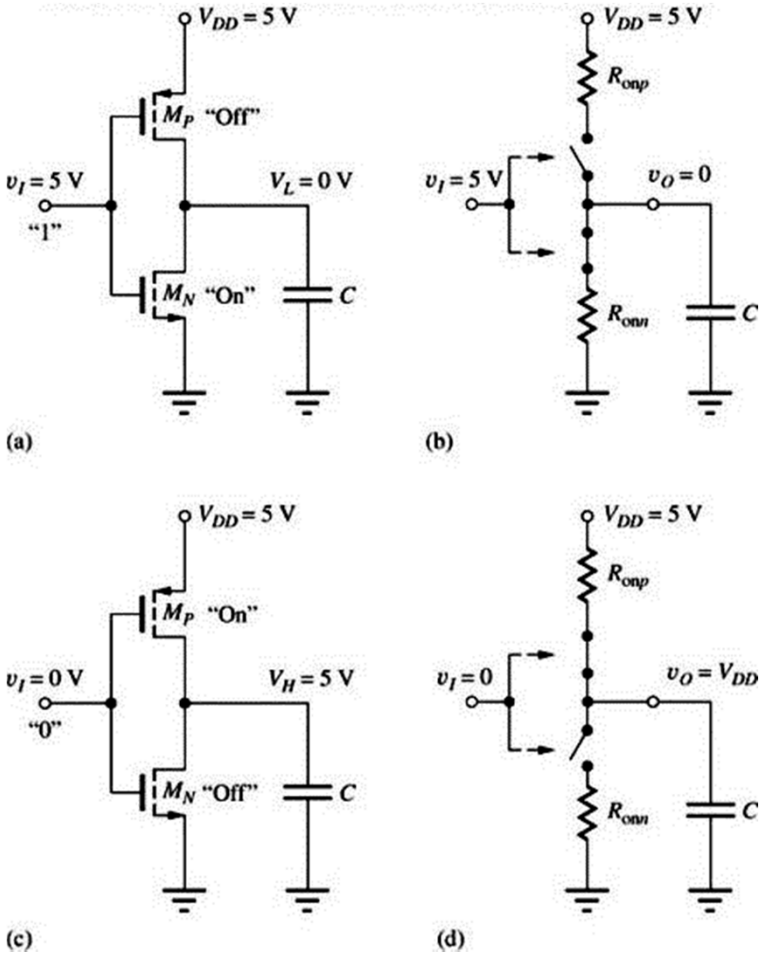


CMOS Inverter – A Switch Model



a) Circuit schematic for a CMOS inverter
b) Simplified operation model with a high input applied
c) Simplified operation model with a low input applied

Static Characteristics of the CMOS Inverter – Switch Model



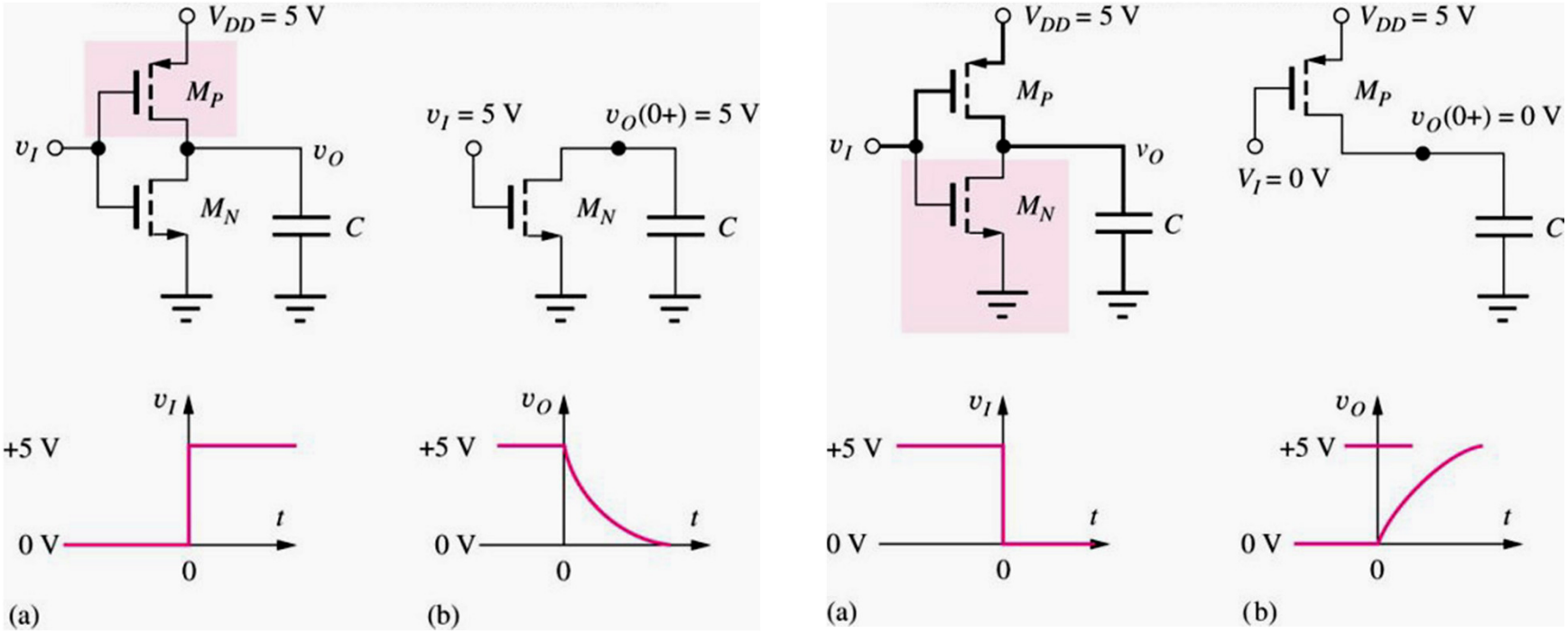
- The figure shows the two modes of static operation with the circuit and simplified models
  - Logic 1 (a) and (b)
  - Logic 0 (c) and (d)
- Notice that $V_H = 5V$ and $V_L = 0V$, and that $I_D = 0A$ which means that there is no static power dissipation

CMOS Inverter Operation

Summarizing:

- When v_I is pulled high (V_{DD}), the PMOS inverter is turned off, while the NMOS is turned on pulling the output down to GND
- When v_I is pulled low (GND), the NMOS inverter is turned off, while the PMOS is turned on pulling the output up to V_{DD}

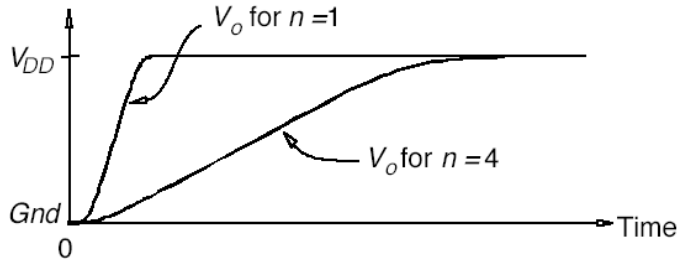
Propagation Delay Estimate



- The two modes of capacitive discharging and charging that contribute to propagation delay

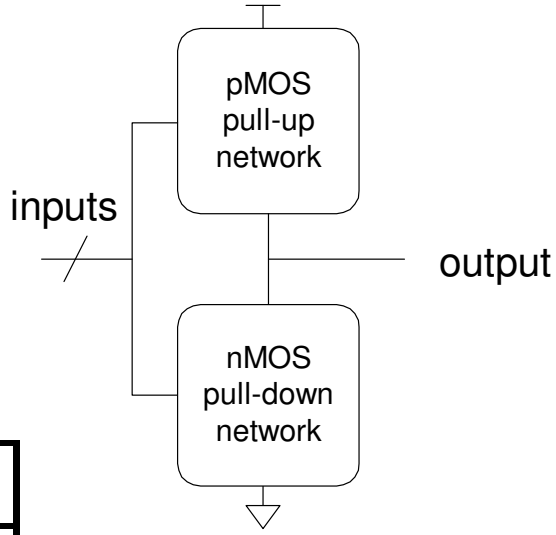
Fan-Out in CMOS Circuits

- While the fan-out of CMOS gates is affected by current limits, the fan-out of CMOS gates driving CMOS gates is enormous since the input currents of CMOS gates is very low.
  - Why are the input currents low?
- On the other hand the high capacitance of CMOS gate inputs means that the capacitive load on a gate driving CMOS gates increases with fan-out.
  - This increased capacitance limits switching speeds and is a far more significant limit on the maximum fan-out.



Complementary CMOS

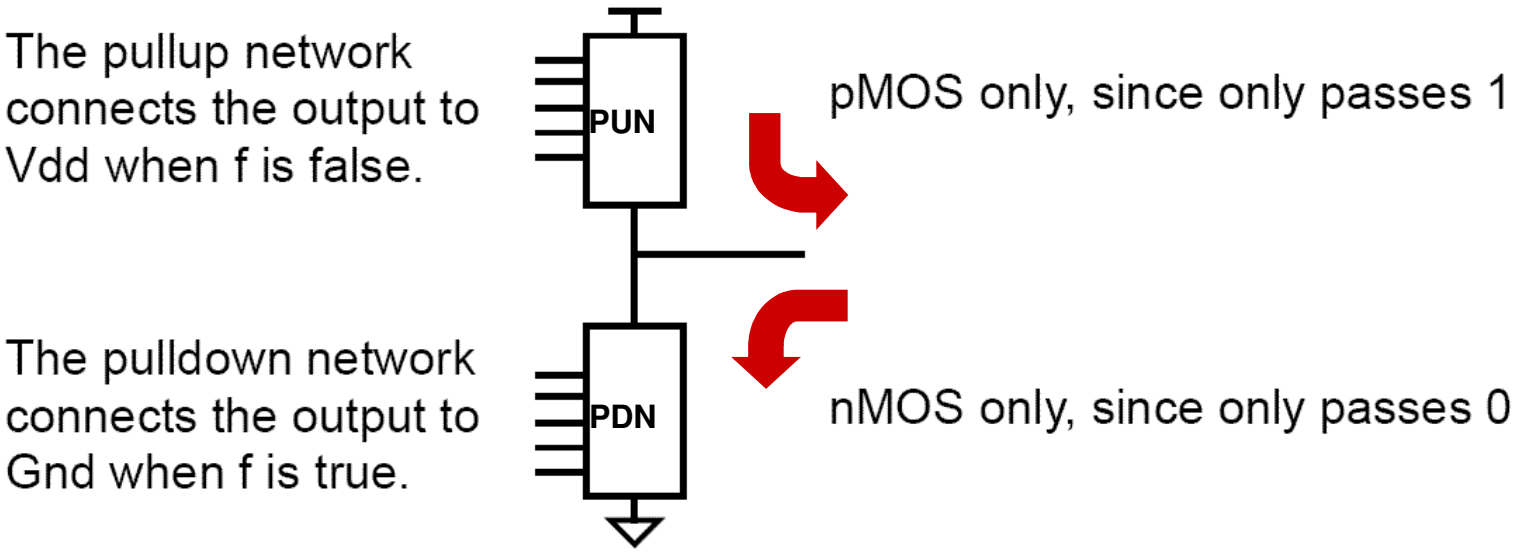
- Complementary CMOS logic gates
  - pMOS *pull-up network*
  - nMOS *pull-down network*
  - a.k.a. static CMOS



	Pull-up OFF	Pull-up ON
Pull-down OFF	Z (float)	1
Pull-down ON	0	X (crowbar)

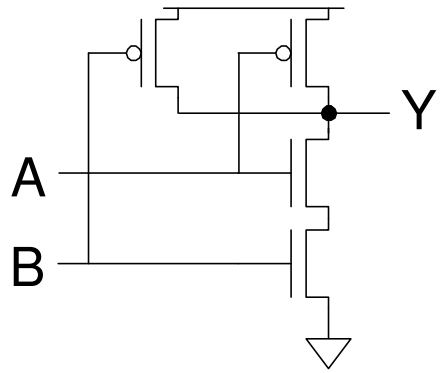
Complementary CMOS

- To build a logic gate we need to build two switch networks:



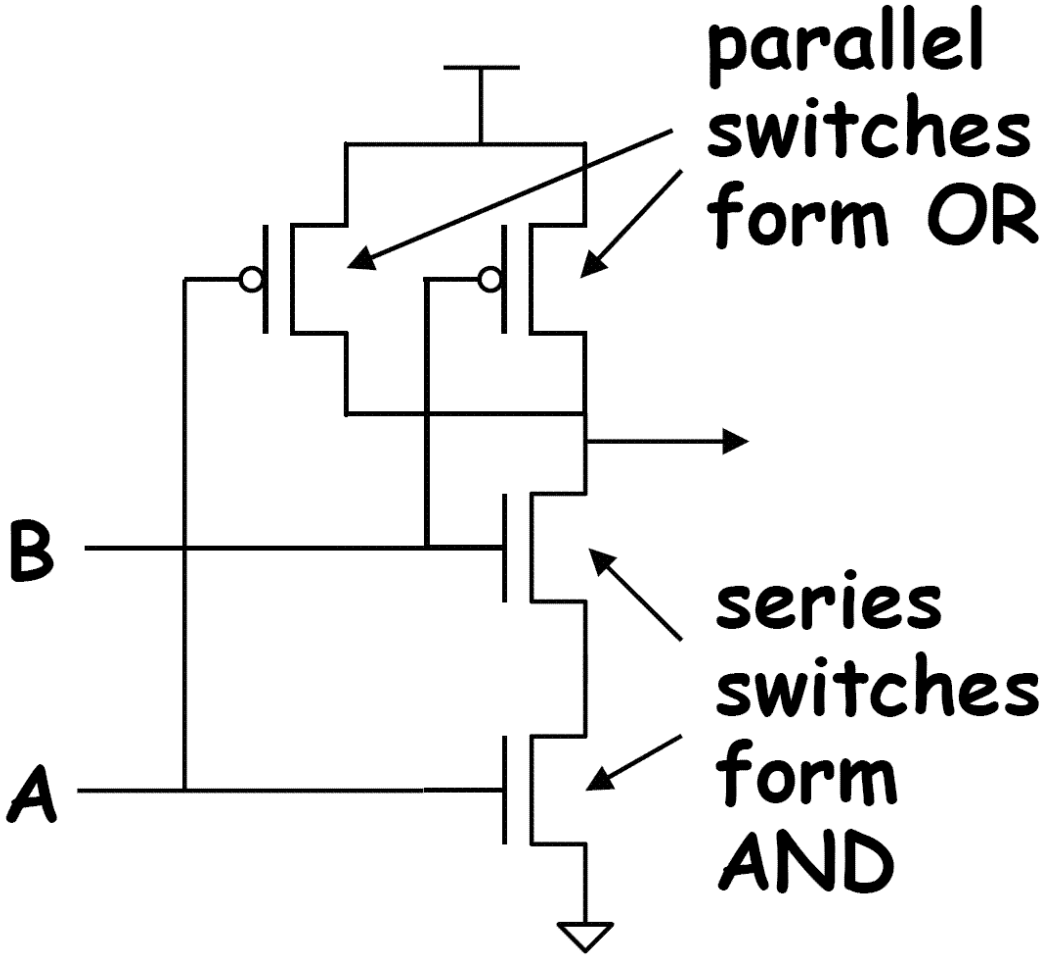
Conduction Complement

- Complementary CMOS gates always produce 0 or 1
- Ex: NAND gate
  - Series nMOS: Y=0 when both inputs are
  - Thus Y=1 when either input is 0
  - Requires parallel pMOS
- Rule of *Conduction Complements*
  - Pull-up network is complement of pull-down
  - parallel → series, series → parallel



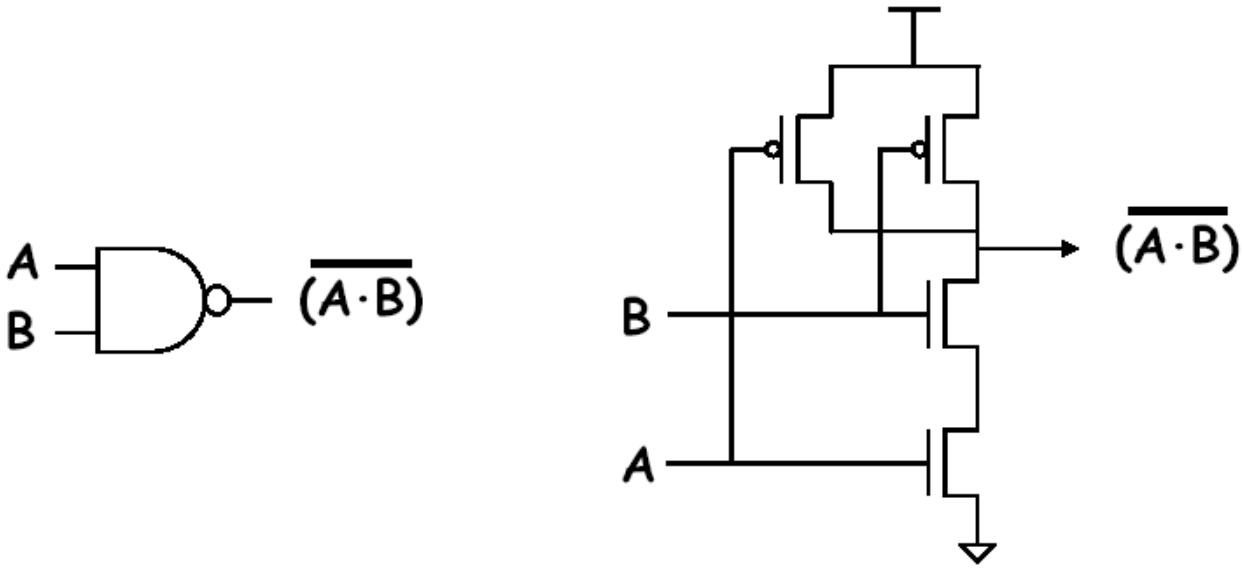
CMOS Gate Design

- Work out the values for both the push and pull networks
- Compare them
- What is the result?



CMOS Gate Design

- A 2-input CMOS NAND gate



CMOS Gate Design

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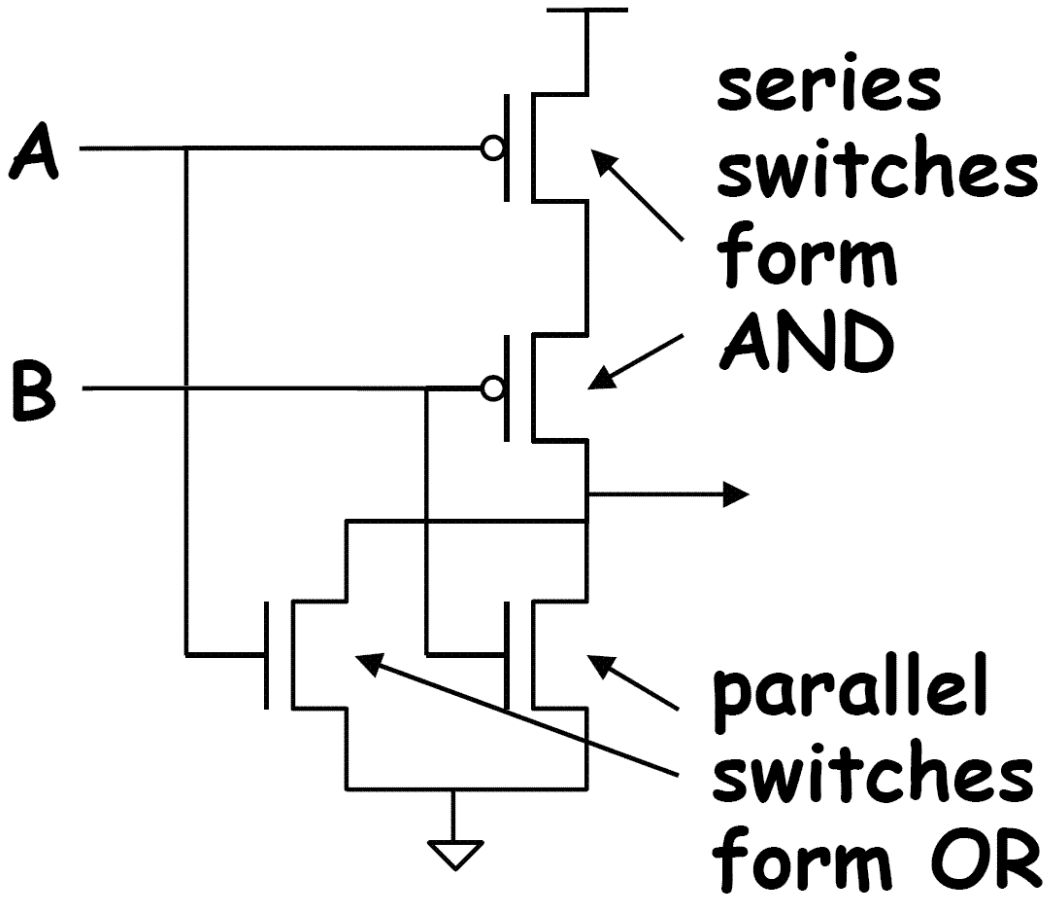
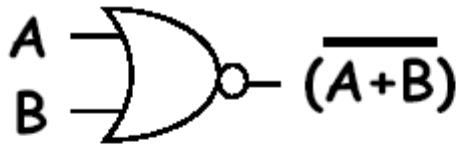
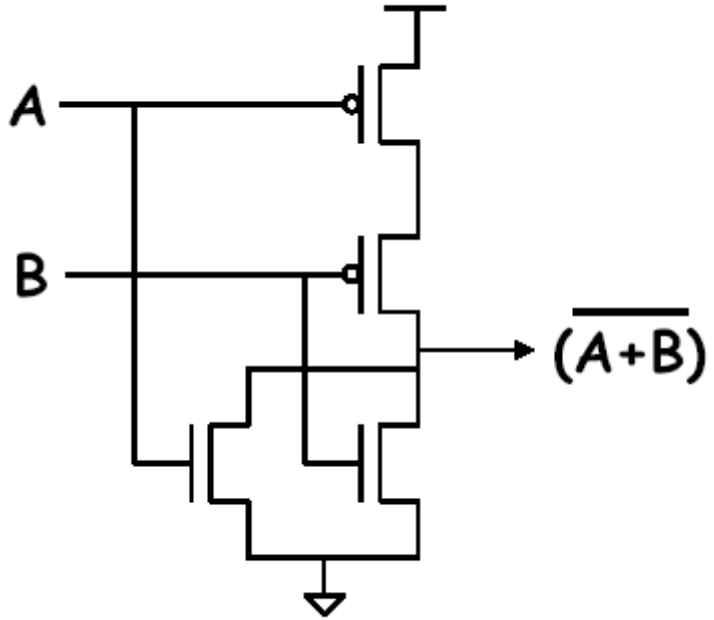


CMOS Gate Design

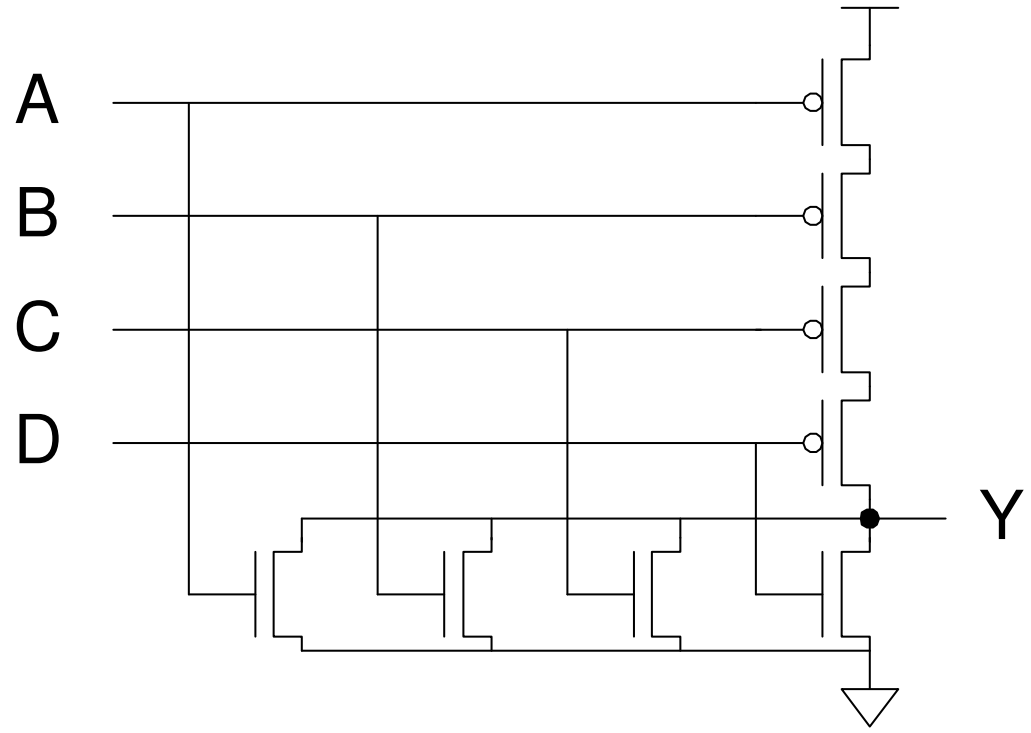
- A 2-input CMOS NOR gate





CMOS Gate Design

- A 4-input CMOS NOR gate

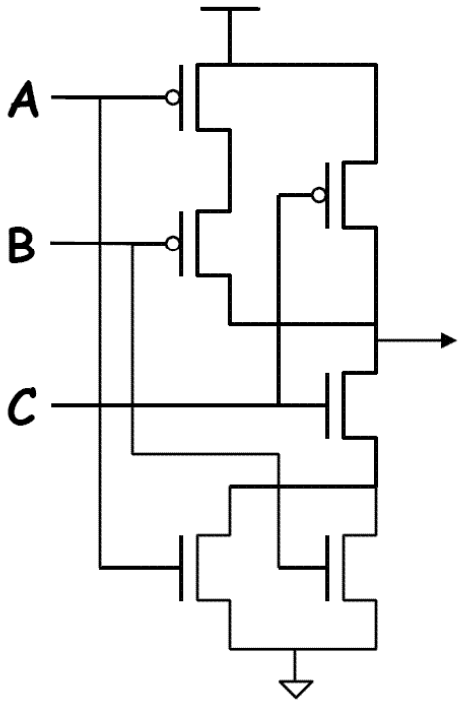


NAND and NOR are Popular

- Logical inversion comes free
  - as a result an inverting gate needs smaller number of transistors compared to the non-inverting one
- In CMOS (and in most other logic families)
  - the simples gates are inverters
  - the next simplest are NAND and NOR gates

Compound Gates

- Lets take a look at a gate that implements a more complex function …



$$f = \overline{(A+B)\cdot C}$$

$$\text{pullup } f = \overline{(A+B)\cdot C}$$

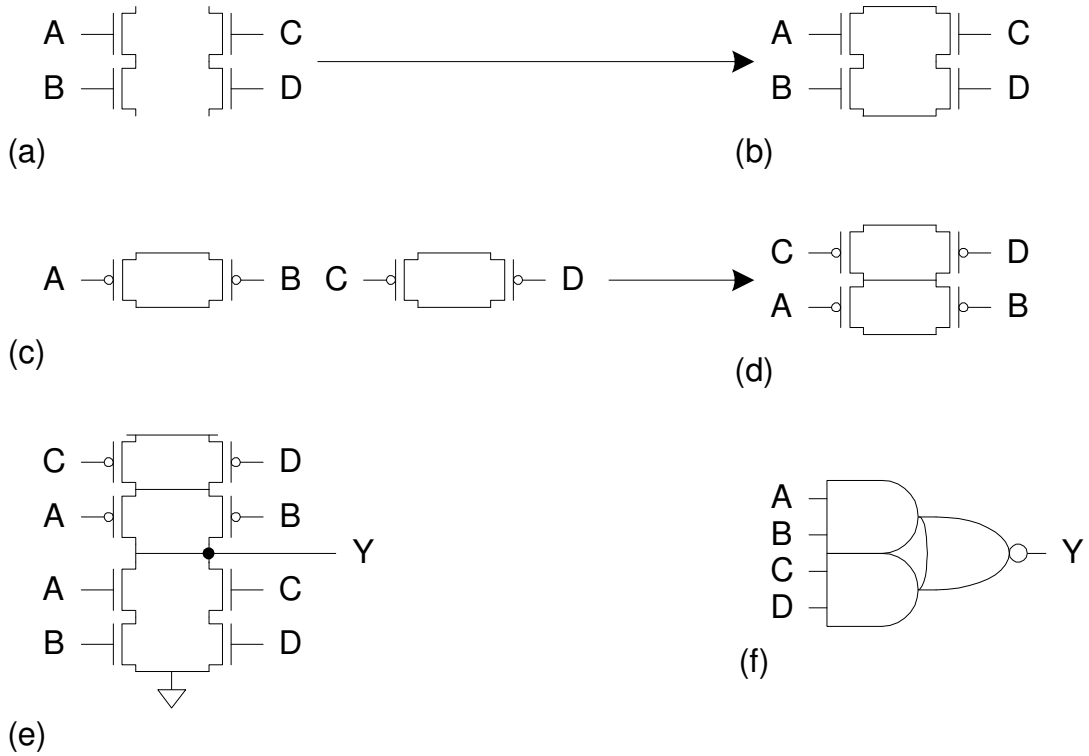
$$= \overline{(\overline{A+B})+\overline{C}}$$

$$= (\overline{\overline{A}\cdot\overline{B}})+\overline{C}$$

$$\text{pulldown } \overline{f} = (A+B)\cdot C$$

Compound Gates

- *Compound gates* can do any inverting function
- Ex: $Y = \overline{A \bullet B + C \bullet D}$



Example: O3AI

- $Y = \overline{(A + B + C) \cdot D}$