Faculty of Engineering

ECE 142: Electronic Circuits

Lecture 12:
MOSFET Large Signal Model

- Based on content from Sedra/Smith “Microelectronic Circuits” - Fifth Edition

MOSFET

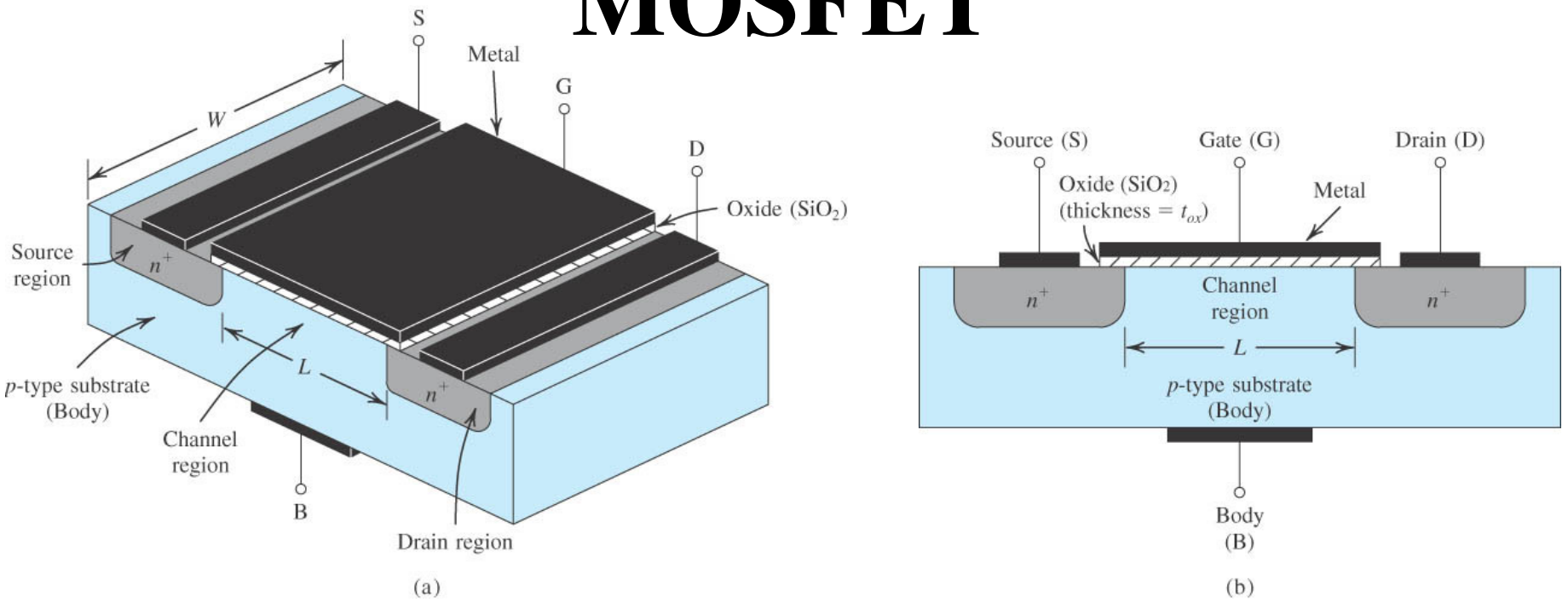


Figure 4.1 Physical structure of the enhancement-type NMOS transistor: **(a)** perspective view; **(b)** cross-section. Typically L = 0.1 to 3 μm, W = 0.2 to 100 μm, and the thickness of the oxide layer (t_{ox}) is in the range of 2 to 50 nm.

Enhancement NMOS

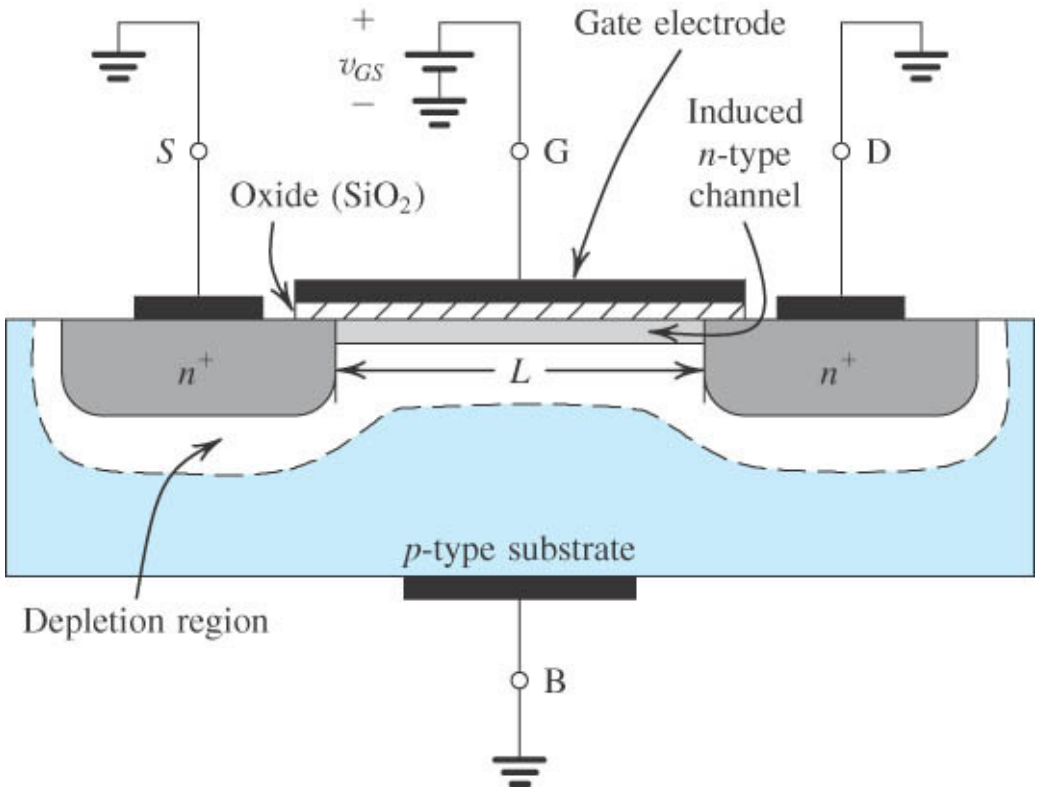


Figure 4.2 The enhancement-type NMOS transistor with a positive voltage applied to the gate. An *n* channel is induced at the top of the substrate beneath the gate.

Linear Mode

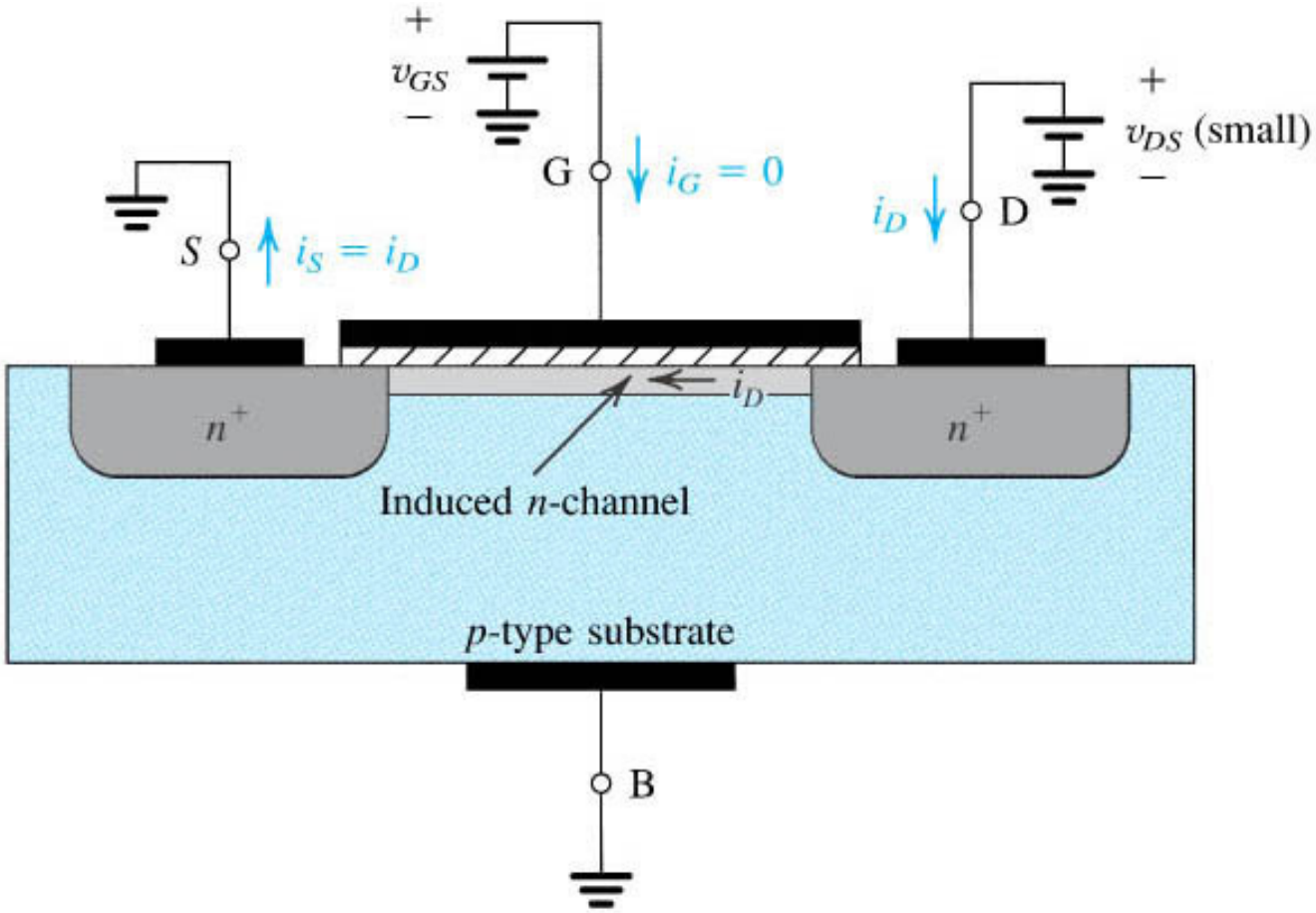


Figure 4.3 An NMOS transistor with $v_{GS} > V_t$ and with a small v_{DS} applied. The device acts as a resistance whose value is determined by v_{GS}. Specifically, the channel conductance is proportional to $v_{GS} - V_t$, and thus i_D is proportional to $(v_{GS} - V_t)\, v_{DS}$. Note that the depletion region is not shown (for simplicity).

I-V Characteristic: Linear Mode

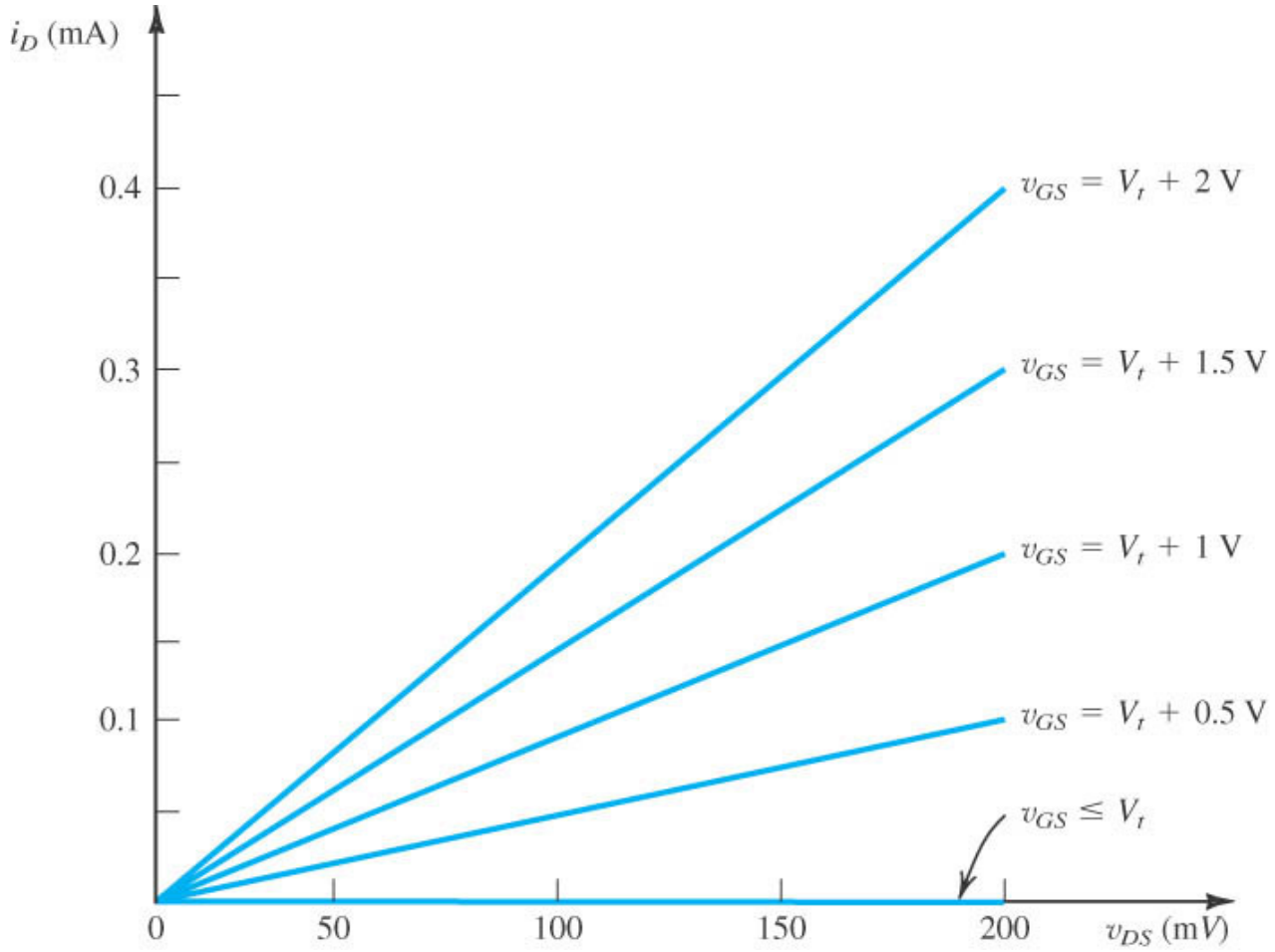


Figure 4.4 The i_D–v_{DS} characteristics of the MOSFET in Fig. 4.3 when the voltage applied between drain and source, v_{DS}, is kept small. The device operates as a linear resistor whose value is controlled by v_{GS}.

Linear Mode (2)

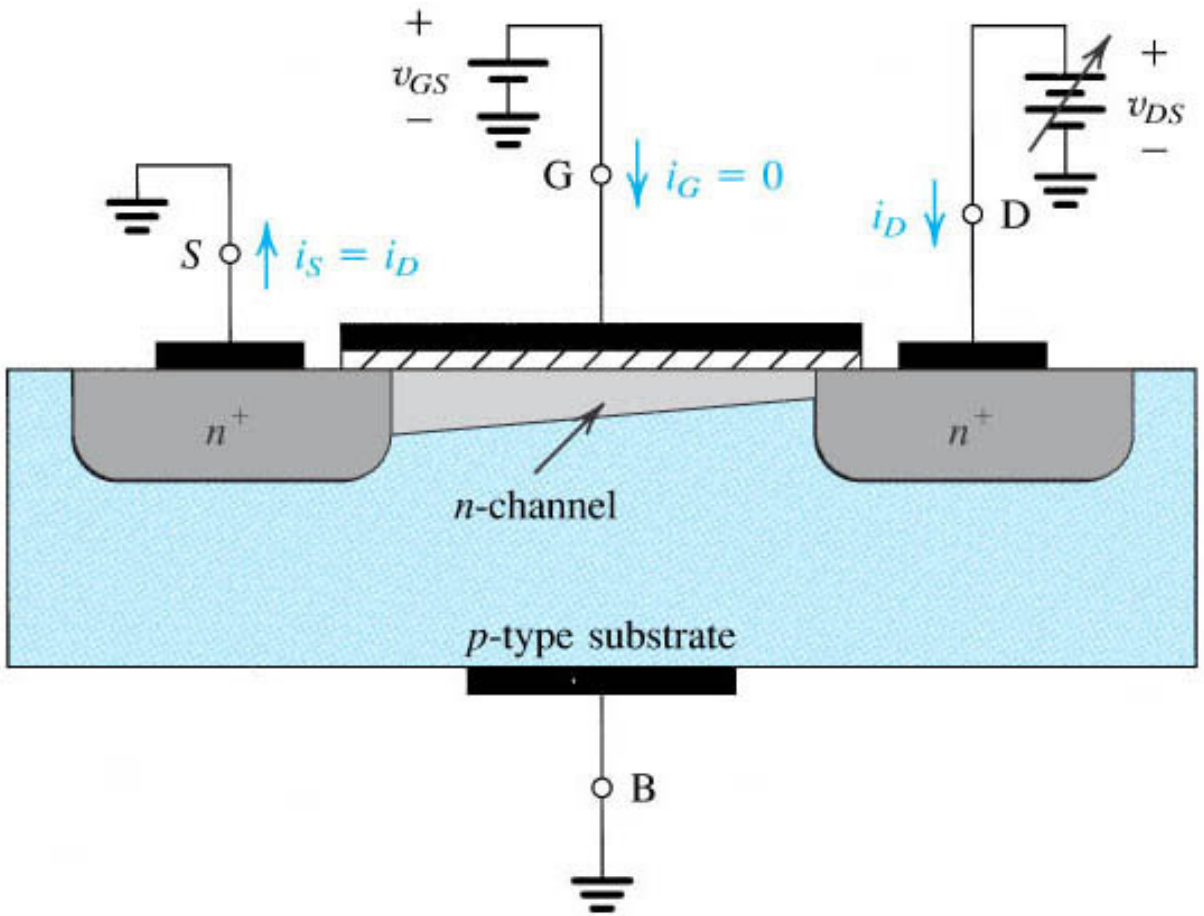


Figure 4.5 Operation of the enhancement NMOS transistor as v_{DS} is increased. The induced channel acquires a tapered shape, and its resistance increases as v_{DS} is increased. Here, v_{GS} is kept constant at a value > V_t.

Ideal I-V Characteristic

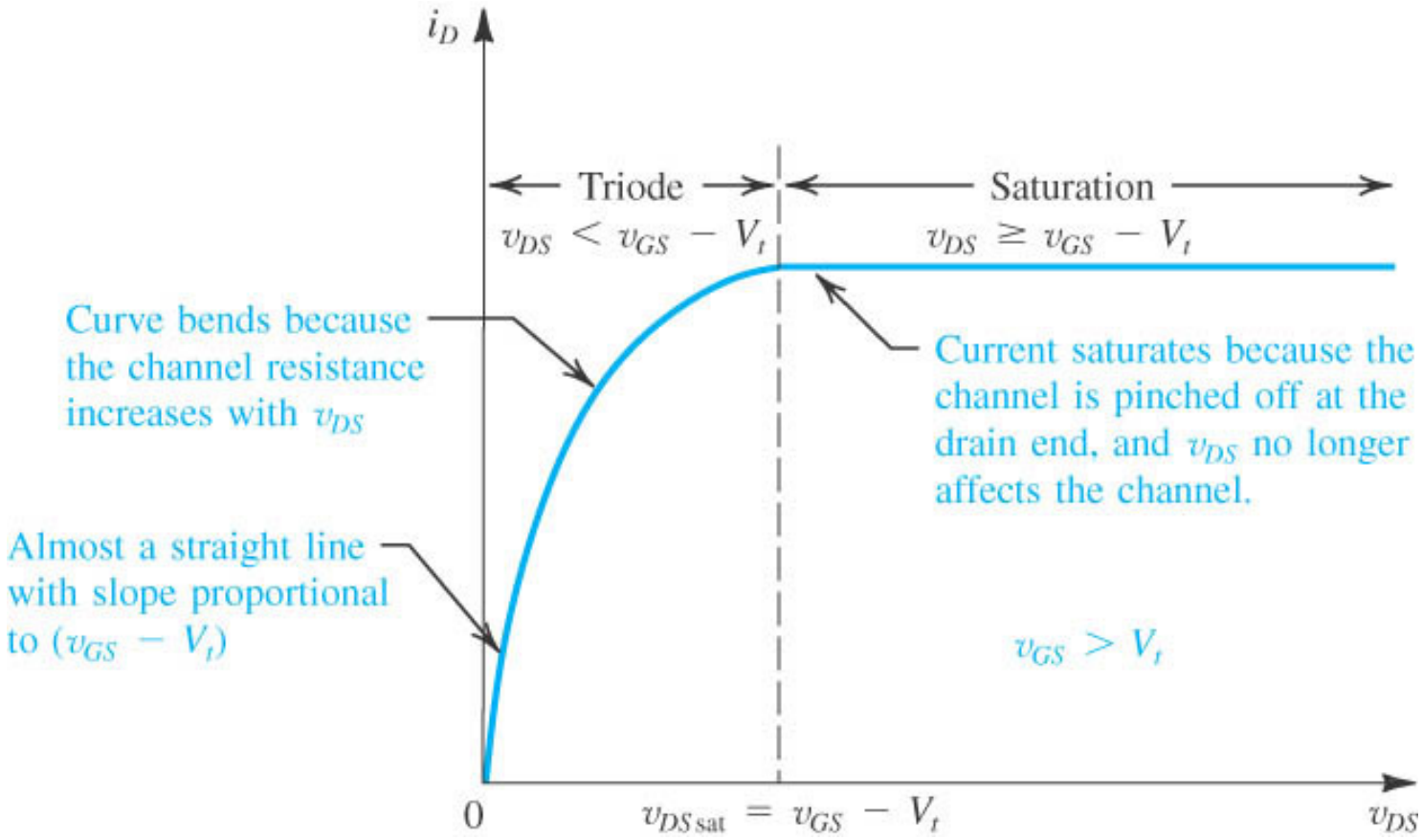


Figure 4.6 The drain current i_D versus the drain-to-source voltage v_{DS} for an enhancement-type NMOS transistor operated with $v_{GS} > V_t$.

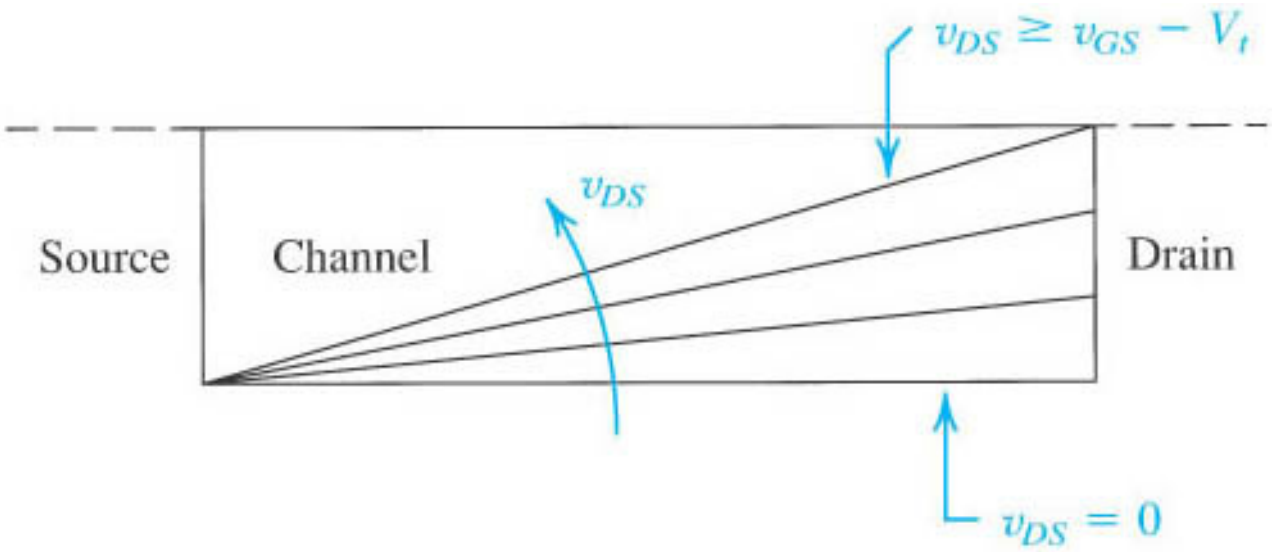


Figure 4.7 Increasing v_{DS} causes the channel to acquire a tapered shape. Eventually, as v_{DS} reaches $v_{GS} - V_t$, the channel is pinched off at the drain end. Increasing v_{DS} above $v_{GS} - V_t$ has little effect (theoretically, no effect) on the channel's shape.

CMOS

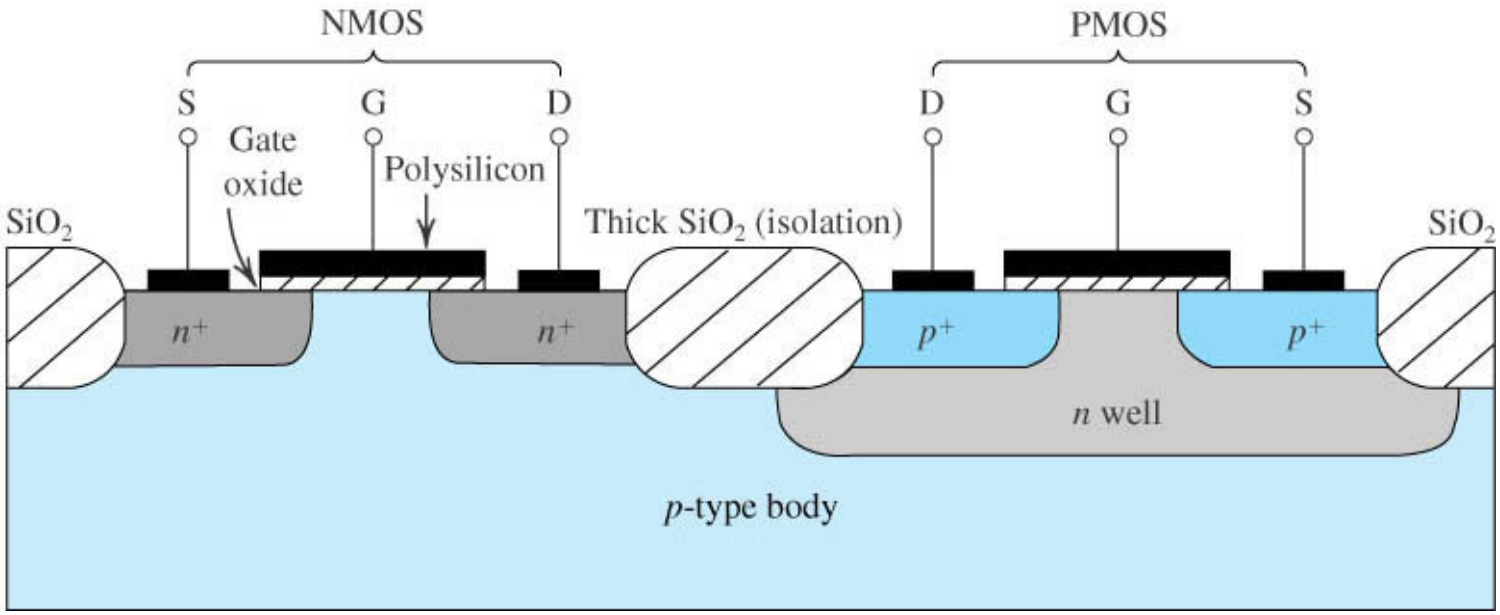


Figure 4.9 Cross-section of a CMOS integrated circuit. Note that the PMOS transistor is formed in a separate *n*-type region, known as an *n* well. Another arrangement is also possible in which an *n*-type body is used and the *n* device is formed in a *p* well. Not shown are the connections made to the *p*-type body and to the *n* well; the latter functions as the body terminal for the *p*-channel device.

Circuit Symbols

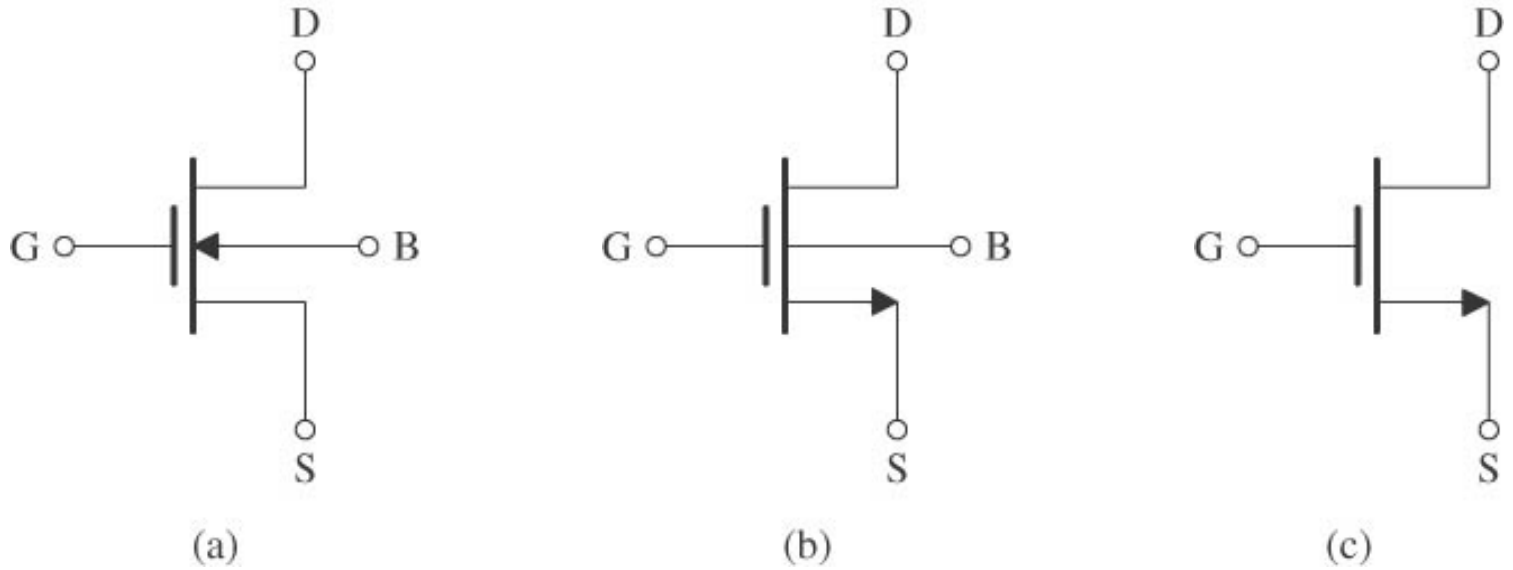


Figure 4.10 **(a)** Circuit symbol for the *n*-channel enhancement-type MOSFET. **(b)** Modified circuit symbol with an arrowhead on the source terminal to distinguish it from the drain and to indicate device polarity (i.e., *n* channel). **(c)** Simplified circuit symbol to be used when the source is connected to the body or when the effect of the body on device operation is unimportant.

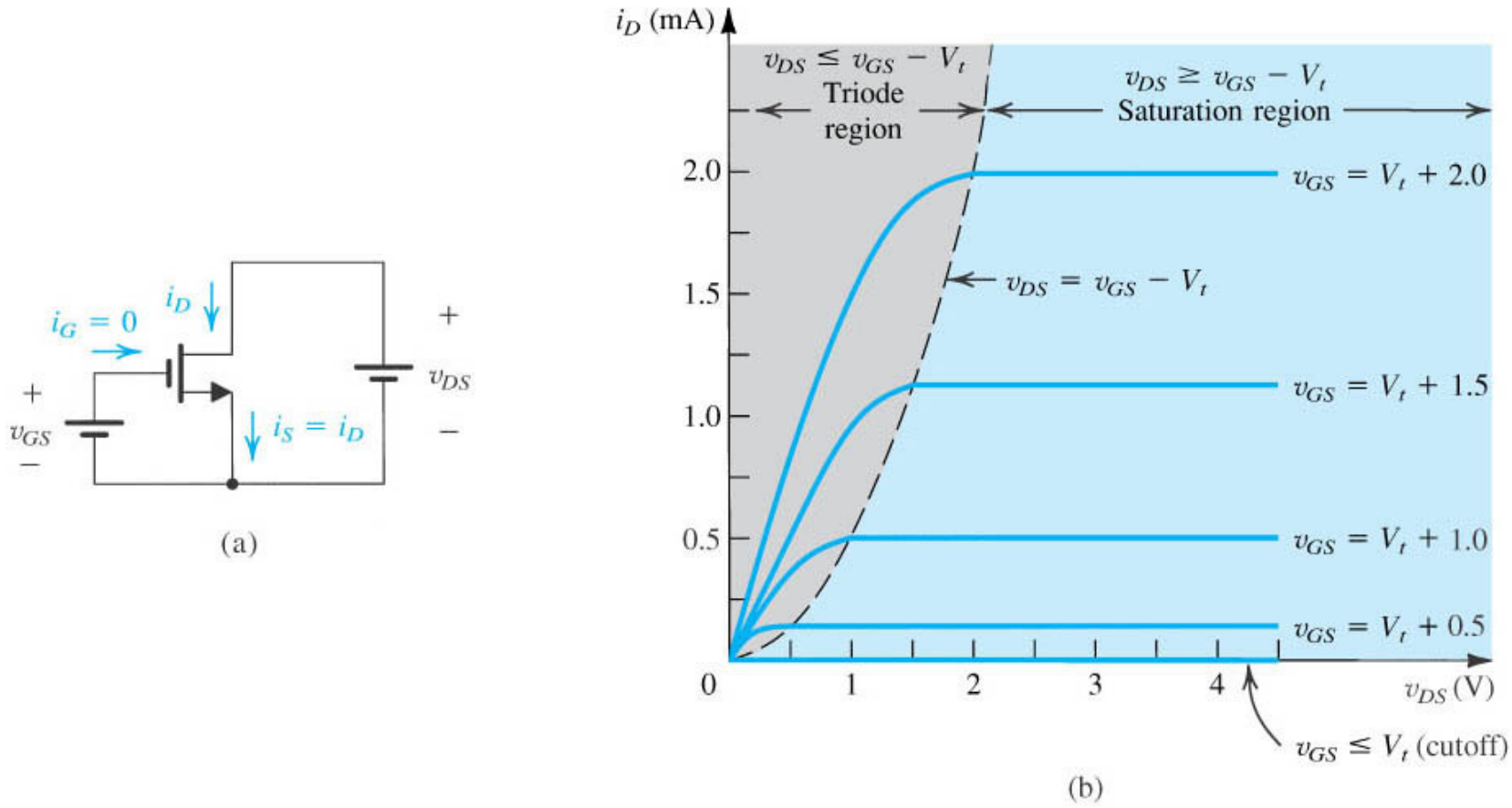


Figure 4.11 **(a)** An *n*-channel enhancement-type MOSFET with v_{GS} and v_{DS} applied and with the normal directions of current flow indicated. **(b)** The i_D–v_{DS} characteristics for a device with $k'_n(W/L) = 1.0$ mA/V^2.

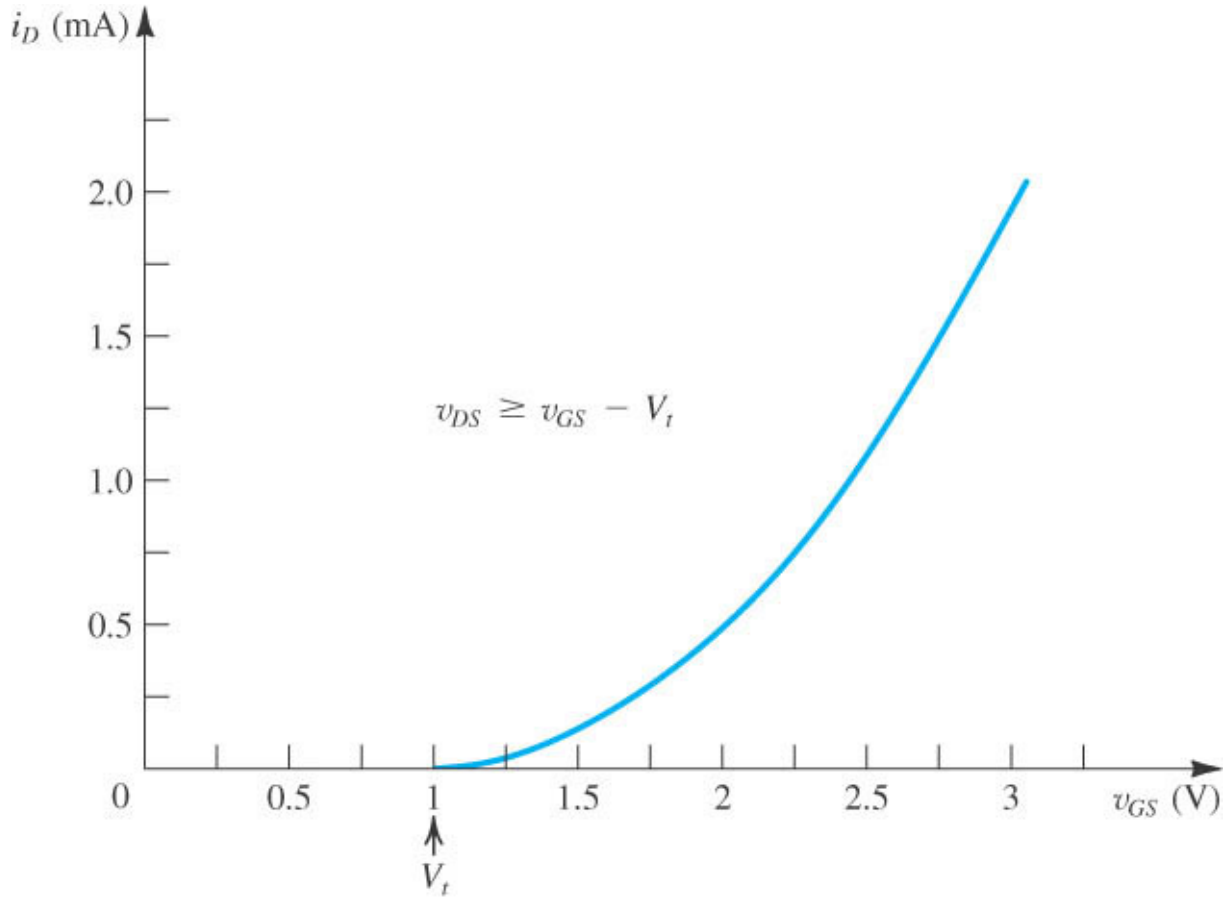


Figure 4.12 The i_D–v_{GS} characteristic for an enhancement-type NMOS transistor in saturation (V_t = 1 V, $k'_n W/L$ = 1.0 mA/V^2).

Large Signal Model

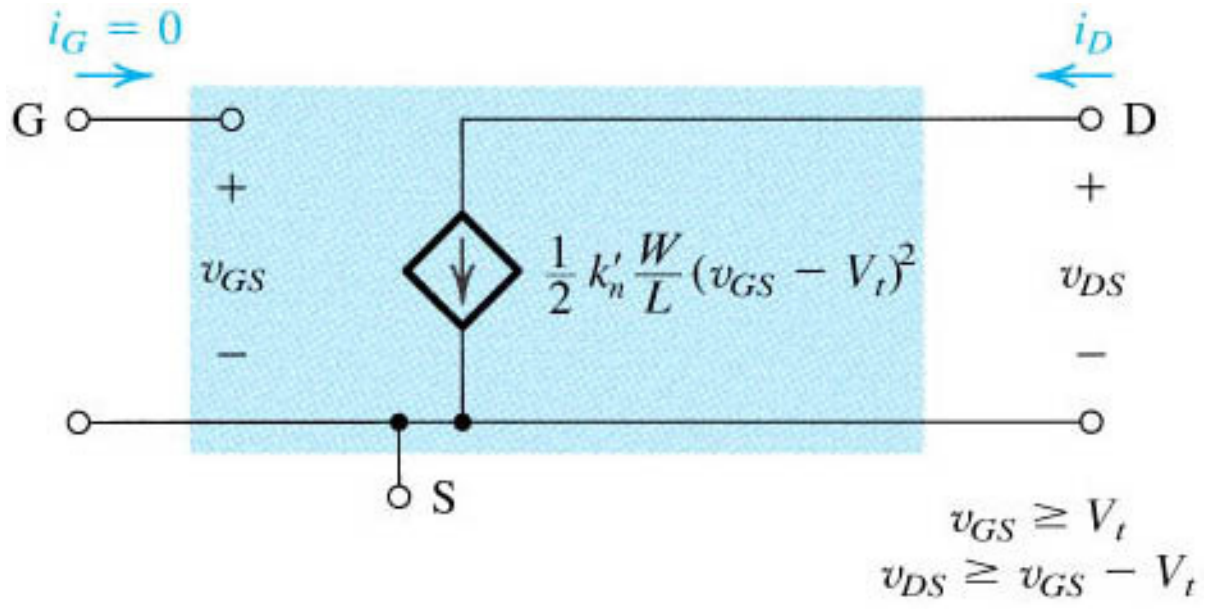


Figure 4.13 Large-signal equivalent-circuit model of an *n*-channel MOSFET operating in the saturation region.

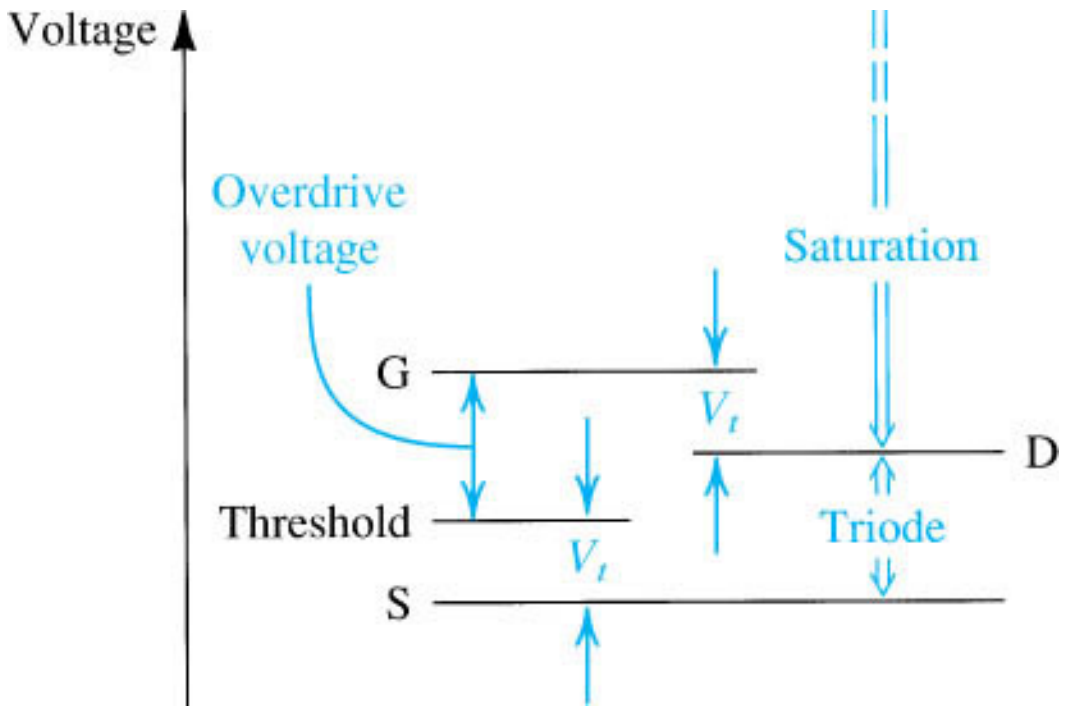


Figure 4.14 The relative levels of the terminal voltages of the enhancement NMOS transistor for operation in the triode region and in the saturation region.

Real I-V Characteristics

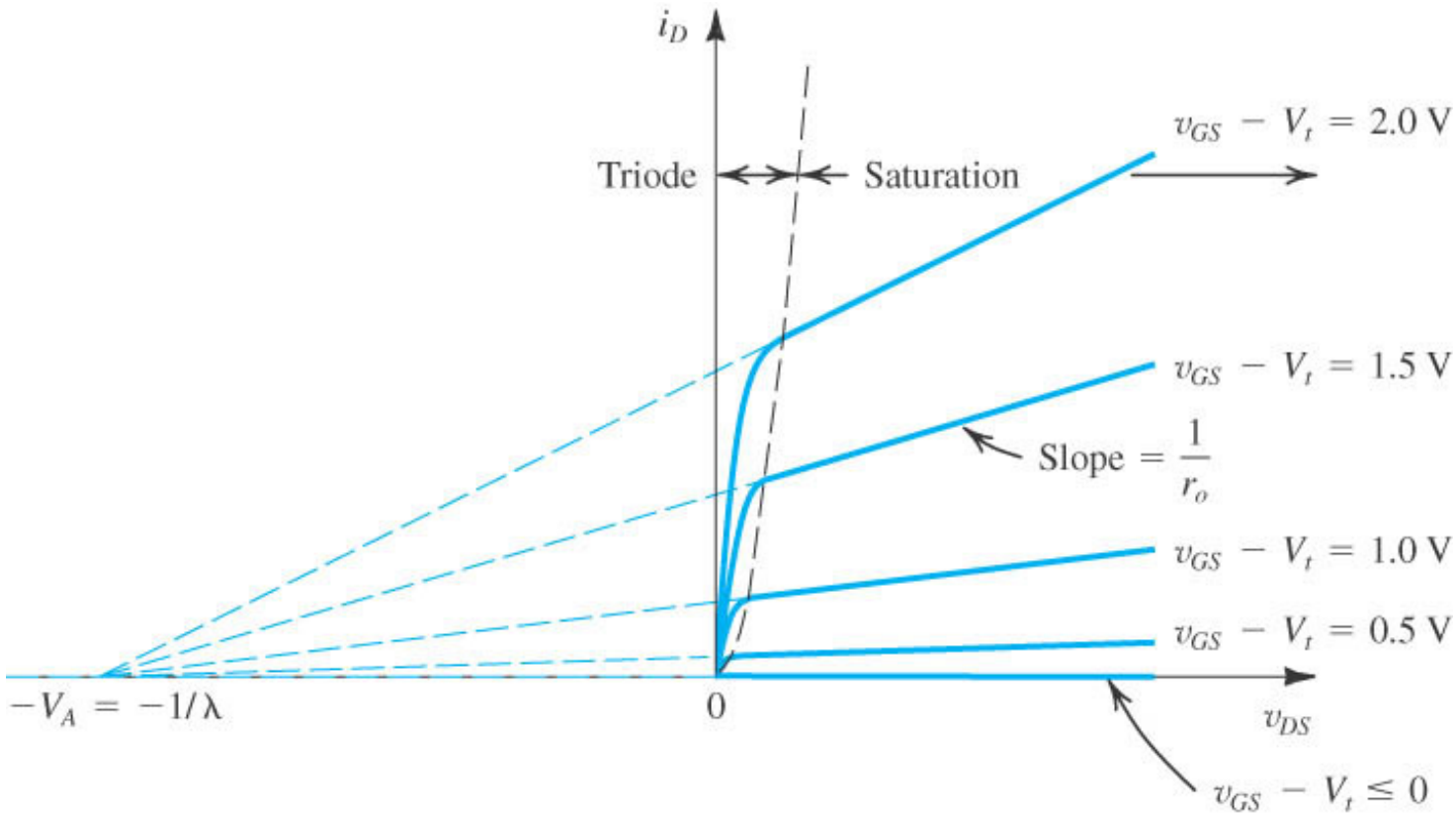


Figure 4.16 Effect of v_{DS} on i_D in the saturation region. The MOSFET parameter V_A depends on the process technology and, for a given process, is proportional to the channel length L.

Modified Large Signal Model

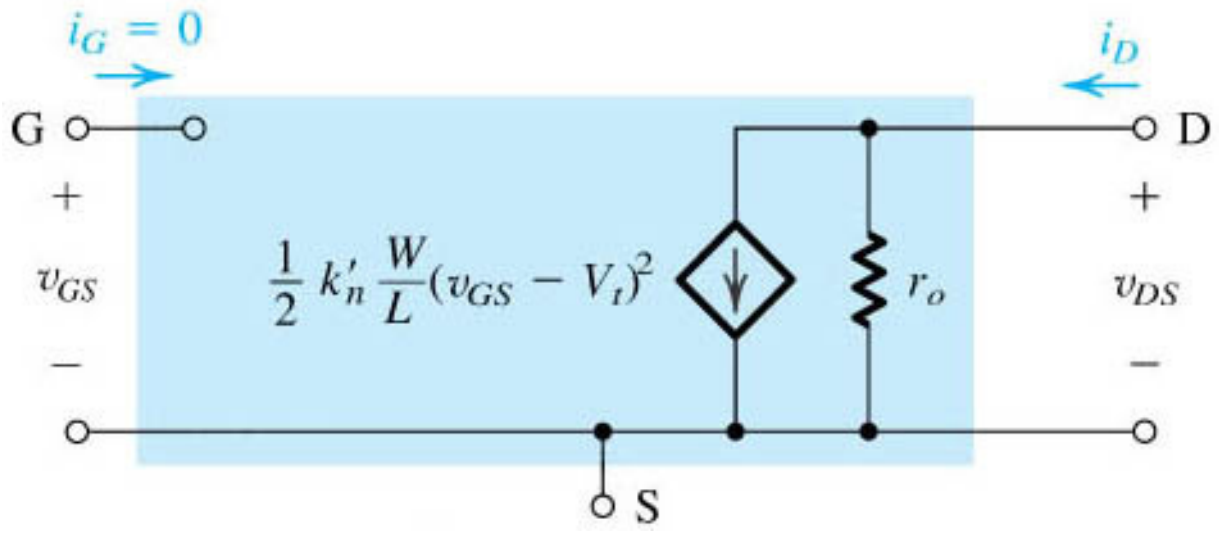


Figure 4.17 Large-signal equivalent circuit model of the *n*-channel MOSFET in saturation, incorporating the output resistance r_o. The output resistance models the linear dependence of i_D on v_{DS} and is given by Eq. (4.22).

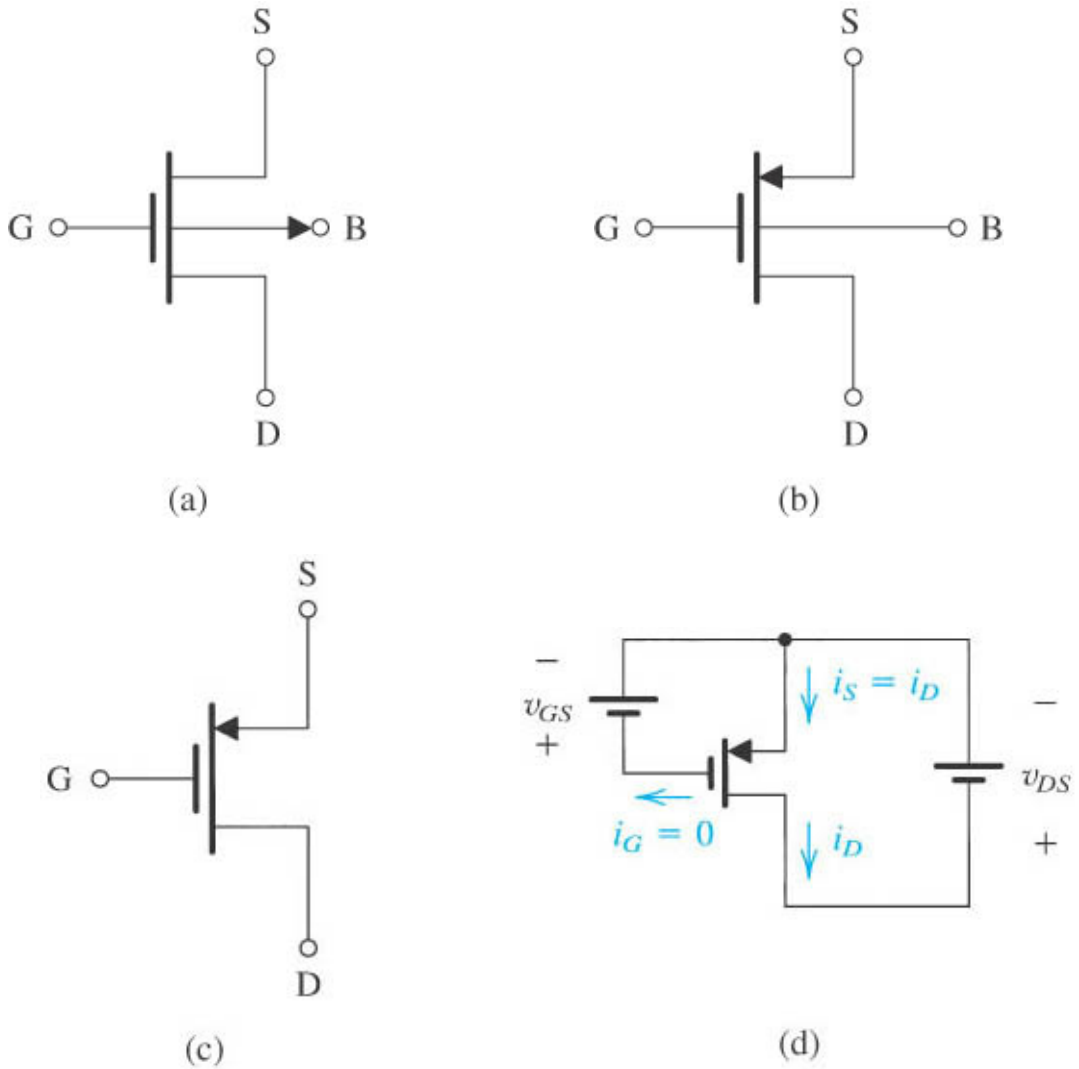


Figure 4.18 **(a)** Circuit symbol for the *p*-channel enhancement-type MOSFET. **(b)** Modified symbol with an arrowhead on the source lead. **(c)** Simplified circuit symbol for the case where the source is connected to the body. **(d)** The MOSFET with voltages applied and the directions of current flow indicated. Note that v_{GS} and v_{DS} are negative and i_D flows out of the drain terminal.

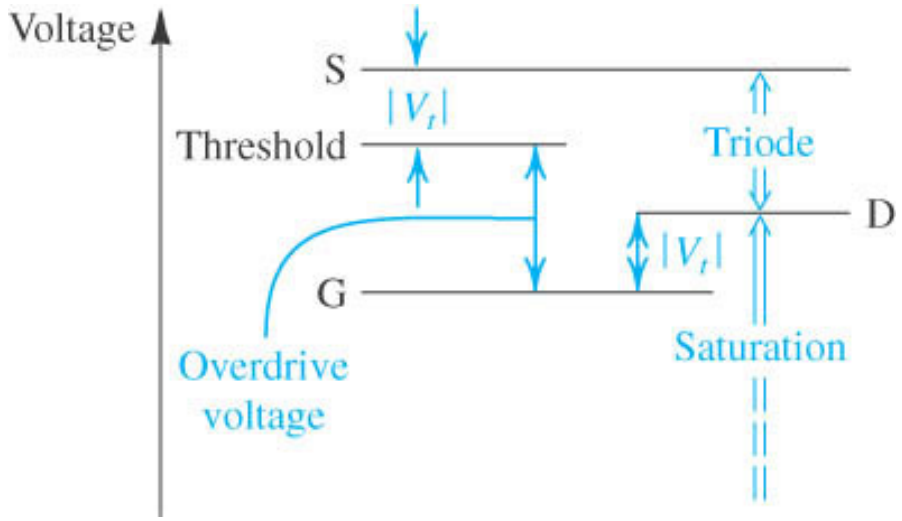
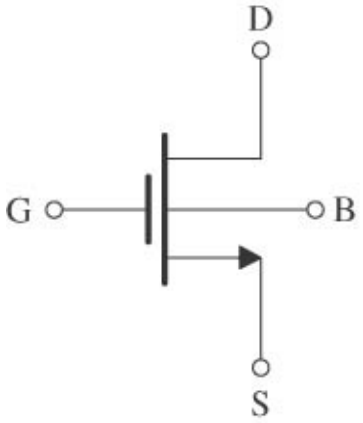
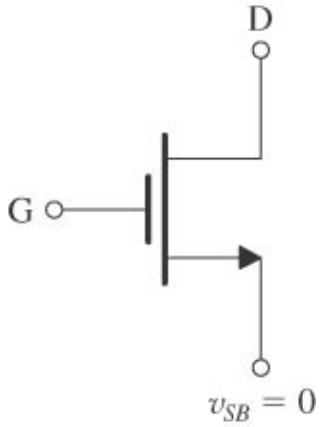
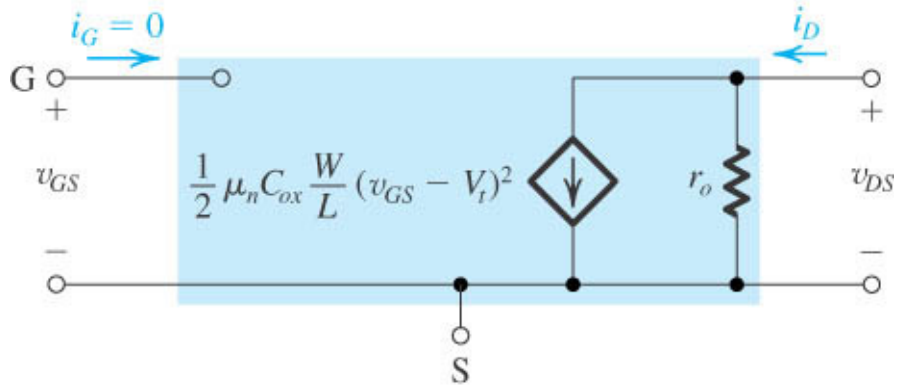


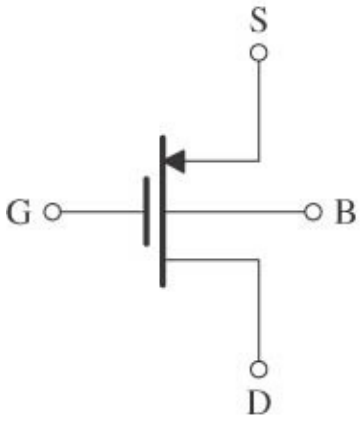
Figure 4.19 The relative levels of the terminal voltages of the enhancement-type PMOS transistor for operation in the triode region and in the saturation region.

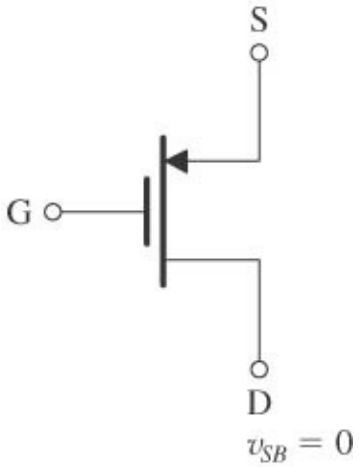
Summary

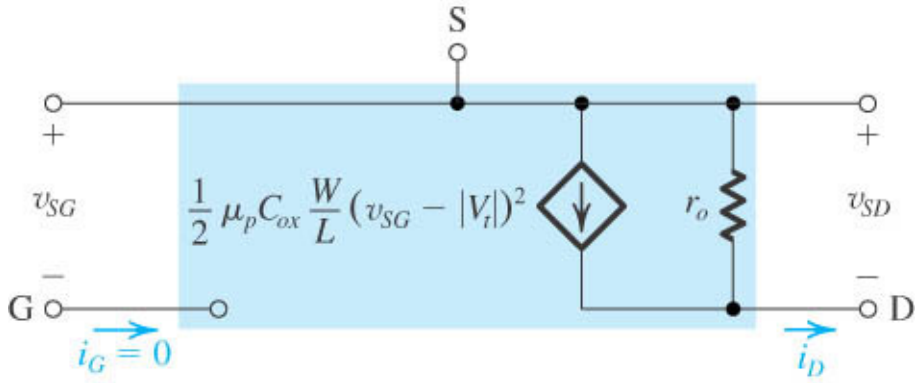

D
G
B
S


D
G
$v_{SB} = 0$


$i_G = 0$
i_D
G
+
v_{GS}
–
$\frac{1}{2}\mu_n C_{ox}\frac{W}{L}(v_{GS} - V_t)^2$
r_o
+
v_{DS}
–
S


S
G
B
D


S
G
D
$v_{SB} = 0$


S
+
v_{SG}
–
G
$i_G = 0$
$\frac{1}{2}\mu_p C_{ox}\frac{W}{L}(v_{SG} - |V_t|)^2$
r_o
+
v_{SD}
–
D
i_D