



Digital logic

Labs 2 and 3

A. Objectives

In this lab the student will learn:

- To use k-maps in simplifying the logic circuits
- Basics of LogiSim software for designing and simulation of logic circuits.
- To implement circuit using 7 segment
- To implement Adder/Subtractor circuit using TTL chips

B. Parts used

- IDL-800 training kit.
- 7408 (Quad 2 i/p AND)
- 7432 (Quad 2 i/p OR)
- 7486 (Quad 2 i/p xor)
- 7448 (BCD to Seven segment decoder)
- 7483 (Four bit full adder)
- Wires
- LogiSim software

C. Introduction

1. Review on Karnaugh map (K-map)

K-map is a method used to simplify Boolean algebra expressions. It consists of 2-dimensional grid where the cells are arranged in Gray code and each cell represents an input combination. K-map replaces the Boolean algebra operations needed in simplification of expressions. This simplification is useful to reduce the number of gates used and the number of inputs used for each gate which results in a reduction in cost and power consumption.

Gray code:

It's binary numeral system at which the two successive values differ in only one bit.

K-map simplification rules:

- Groups may not include any cell contain a zero.
- Groups may be horizontal or vertical but not diagonal.
- Groups must contain 2^n number of cells (1,2,4,8 ...).
- Each group should be as large as possible.
- Each cell containing a "1" should be in at least one group.
- Groups may overlap.
- Groups may wrap around the table (The leftmost cell in a row may be grouped with the rightmost cell and also the uppermost can be grouped with the lower most).
- There should be as few groups as possible.

Table 1: Gray code

2-bit	4-bit
00	0000
01	0001
11	0011
10	0010
3-bit	0110
000	0111
001	0101
011	0100
010	1100
110	1101
111	1111
101	1110
100	1010
	1011
	1001
	1000



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2. Introduction to LogiSim software

LogiSim is a free open source software used in designing and simulating logic circuits.

The main two sections of the program's interface are the components section (Number 1) where you can add any logic component you will need in the design. The other section is the toolbar (Number 2) which contains the hand tool that changes the input values within the circuit, the edit tool that edits the gates position and make wiring, the text tool to add your comments on the design and icons for adding input or output pins.

3. Seven segment Display

A seven-segment display displays decimal numbers. It consists of seven Light Emitting Diodes (LEDs), which are arranged to form different digits as shown in Figure 1. The seven segment displays come in two forms: Common Anode (CA) and Common Cathode (CC). A common anode 7-segment display has all of the anodes tied together while a common cathode 7-segment display has all the cathodes tied together. By turning ON and OFF LEDs, a decimal digit can be displayed. For example, for a common Cathode 7-segment display connecting b & c to the VCC (logic 1) and connect the rest of inputs to ground (logic 0) would display the decimal digit 1.

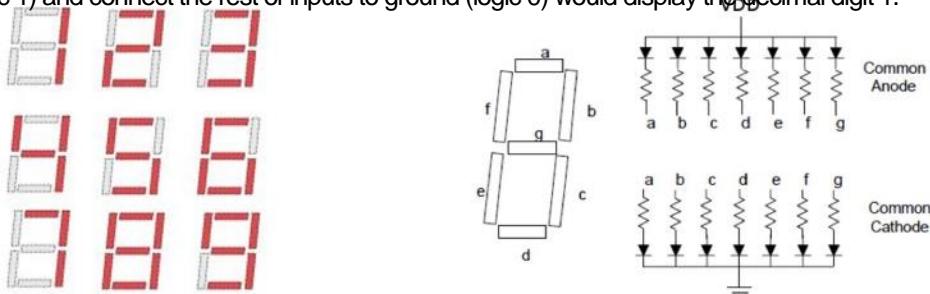


Figure 1

The IDL-800 provides two 7-segment displays. The displays are connected to a binary to 7 segment decoder. The binary numbers 0000-1001 (0-9) may be displayed by providing binary numbers on the input connections labeled A through D. The sequence of inputs is reversed from standard notation with A being the least significant bit and D the most significant (i.e. DCBA). The connection labeled P activates the decimal point. GND must be applied to D1 to activate the right display, and to D2 to activate the left one.

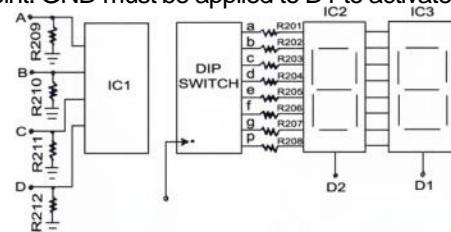


Figure 2

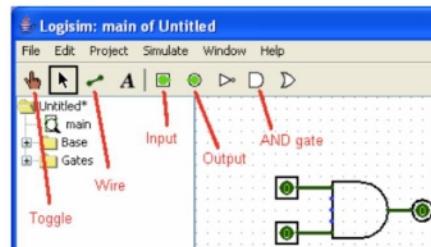
**D. Experiments****1. Getting hands on LogiSim**

Figure 3

- Select the AND gate from the toolbar in Fig. 3 and place the gate in the dotted field.
- Select the Input tool, and place two inputs to the left of the AND gate. Click on the number next to "Number of Inputs" and change it to 2.
- Add a label to your AND gate by clicking the blank field next to "Label" in the properties pane.
- Select the Output tool, and place one output to the right of the AND gate.
- Select the Wire tool, and draw a wire connecting the two inputs to the input pins of the AND gate. Also connect the output to the output pin of the AND gate.
- Use the Toggle tool to change the values of the inputs while observing the output.

Selection: AND Gate	
Facing	East
Data Bits	1
Gate Size	Wide
Number Of Inputs	5
Output Value	0/1
Label	
Label Font	SansSerif Plain 12
Negate 1 (Top)	No
Negate 2	No
Negate 3	No
Negate 4	No
Negate 5 (Bottom)	No

2. Simplify and Verify with implementation the following Boolean expression $X = A \cdot B + A \cdot C + B + BC$

- Implement the expression using the TTL chips without simplifying. Record the results in Table 1.

A	B	C	X	Simplified expression	Check
0	0	0			
0	0	1			
0	1	0			
0	1	1			
1	0	0			
1	0	1			
1	1	0			
1	1	1			

- Simplify the expression using k-map technique, Simulate the simplified version using LogiSim and Compare the results

A 0 1	B 0 C 1	00	01	11	10



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3. Implementation of 2-bit Adder/Subtractor circuit

- a) Design a 1-bit Full Adder (FA) circuit starting from the truth table.

Inputs			Outputs	
Cin	X	Y	S	Cout

\diagup				

\diagup				

- b) Draw the block diagram of a 2-bit adder circuit

- c) Implement the Circuit using TTL chips on the Digital Trainer kit display the output on LEDs d)
Display the output on the 7-segment display.
e) Draw the Pin-to-Pin diagram of your circuit on the Logisim using the 7400-Lib then modify it to act as
Adder/Subtractor circuit with add/sub signal (1: subtracts,0:adds) (you may use 7483 chip)