Digital Design

Sheet 5

1) Show how to build each of the following single- or multiple-output logic functions using one or more 74x138 or 74x139 binary decoders and NAND gates.
(Hint: Each realization should be equivalent to a sum of minterms.)

a) $F = \Sigma_{X,Y,Z}(2,4,7)$
b) $F = \prod_{A,B,C}(3,4,5,6,7)$
c) $F = \Sigma_{A,B,C,D}(2,4,6,14)$
d) $F = \Sigma_{W,X,Y,Z}(0,1,2,3,5,7,11,13)$
e) $F = \Sigma_{W,X,Y}(1,3,5,6)$
f) $F = \Sigma_{A,B,C}(0,4,6)$
g) $G = \Sigma_{W,X,Y}(2,3,4,7)$
h) $G = \Sigma_{C,D,E}(1,2)$

2) Draw the digits created by a 74x49 seven-segment decoder for the non-decimal inputs 1010 through 1111.

3) a. A possible definition of a BUT gate (Exercise 4.45) is "Y1 is 1 if A1 and B1 are 1 but either A2 or B2 is 0; Y2 is defined symmetrically." Write the truth table and find minimal sum-of-products expressions for the BUT-gate outputs. Draw the logic diagram for a NAND-NAND circuit for the expressions, assuming that only uncomplemented inputs are available. You may use gates from 74HCT00, '04, '10, '20, and '30 packages.

b. Find a gate-level design for the BUT gate defined in Exercise 5.31 that uses a minimum number of transistors when realized in CMOS. You may use gates from 74HCT00, '02, '04, '10, '20, and '30 packages. Write the output expressions (which need not be two-level sums-of-products), and draw the logic diagram

4) a. Suppose that you are asked to design a new component, a decimal decoder that is optimized for applications in which only decimal input combinations are expected to occur. How can the cost of such a decoder be minimized compared to one that is simply a 4-to-16 decoder with six outputs removed? Write the logic equations for all ten outputs of the minimized decoder, assuming active-high inputs and outputs and no enable inputs.

b. How many Karnaugh maps would be required to work Exercise (a) using the formal multiple-output minimization procedure described in Section 4.3.8?

5) Redesign the MSI 74x49 seven-segment decoder so that the digits 6 and 9 have tails. Are any of the digit patterns for non-decimal inputs 1010 through 1111 affected by your redesign?

6) Write the truth table and a logic diagram for the logic function performed by the CMOS circuit in Figure 5.1. (The circuit contains transmission gates, which were introduced in Section 3.7.1.)

7) A 16-bit barrel shifter is a combinational logic circuit with 16 data inputs, 16 data outputs, and 4 control inputs. The output word equals the input word, rotated by a number of bit positions specified by the control inputs. For example, if the input word equals ABCDEFGHIJKLMNOP (each letter represents one bit), and the control inputs are 0101 (5), then the output word is FGHIJKLMNOPABCDE. Design a 16-bit barrel shifter using combinational MSI parts discussed in this chapter. Your design should contain 20 or fewer ICs. Do not draw a complete schematic, but sketch and describe your design in general terms and indicate the types and total number of ICs required.

8) What logic function is performed by the CMOS circuit shown in Figure 5.2?

9) Write the truth table and a logic diagram for the logic function performed by the CMOS circuit in Figure 5.3.

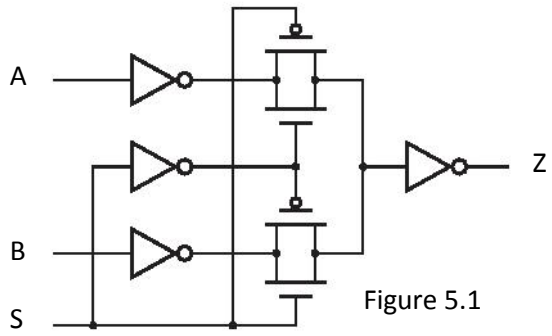

Figure 5.1

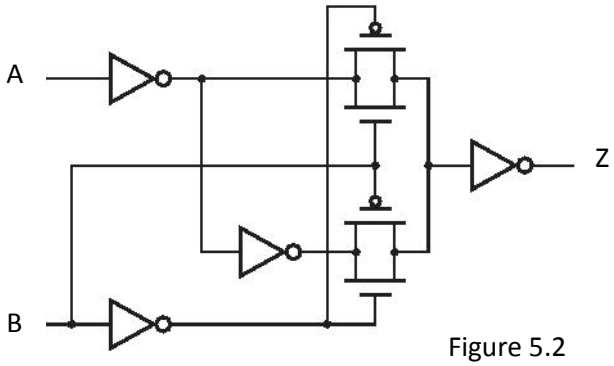

Figure 5.2

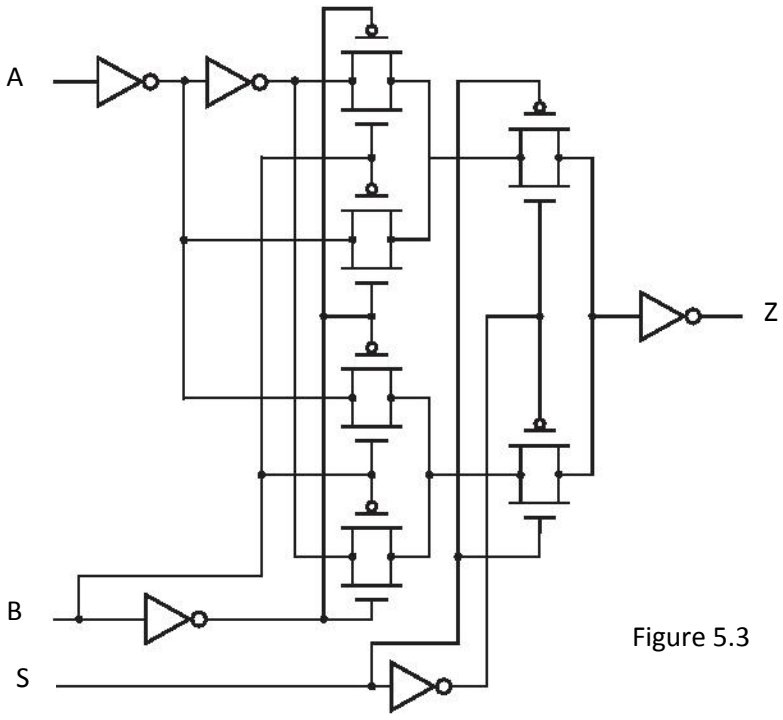

Figure 5.3