Faculty of Engineering

CSE115: Digital Design

Lecture 24:
State Machines

Suggested Reading

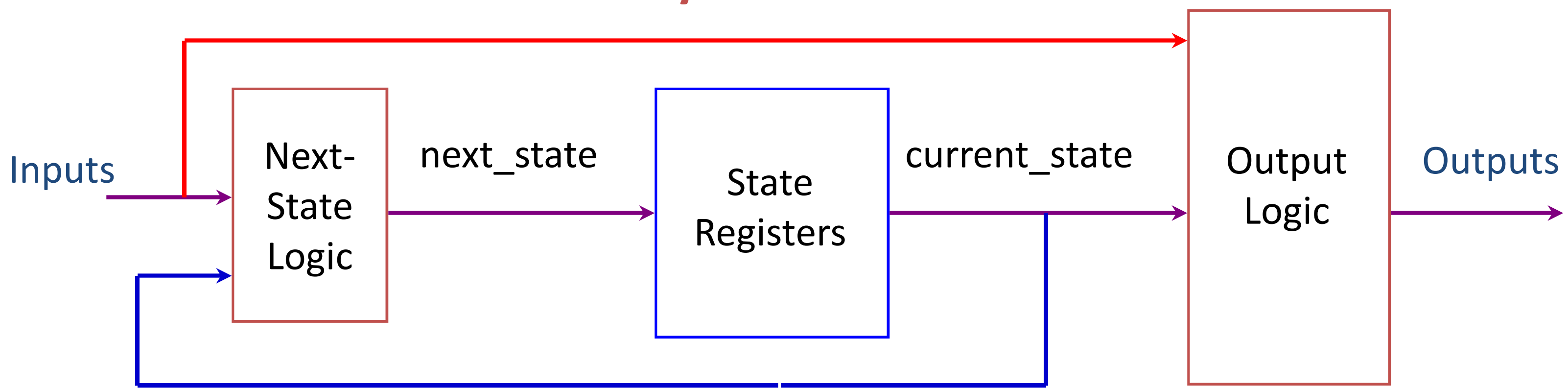
- Sections 7.3-7.6

Clocked Synch State-Machine Analysis

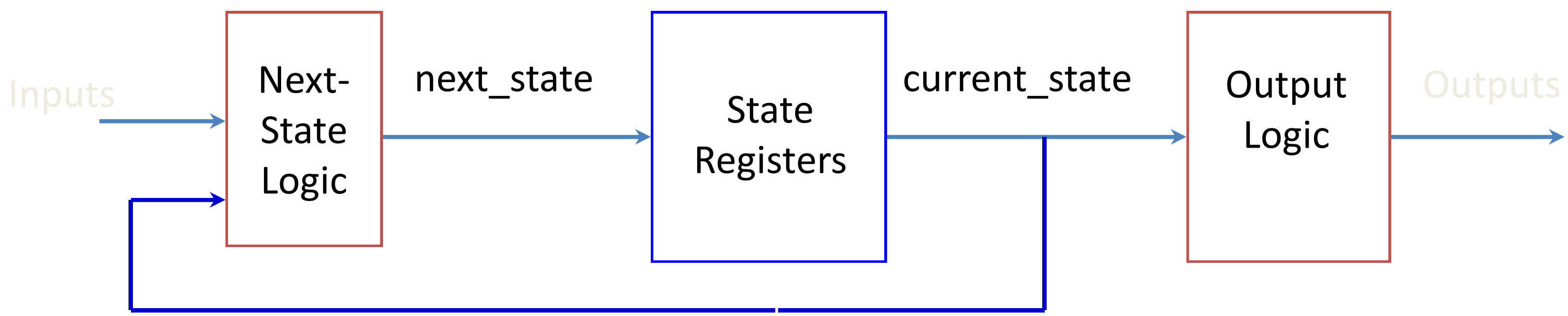
- **Analysis**
  - How does a given circuit work? What does it do?
  - How do input sequences map to output sequences?
- **Mealy Machine**
  - Next state = F (current state, inputs)
  - **Output** = G (current state, inputs)
- **Moore Machine**
  - Next state = F (current state, inputs)
  - **Output** = G (current state)

Diff between Mealy & Moore Machines

Mealy Machine



Moore Machine



Basic Analysis of State Machines

1. Determine **next-state** and **output** **functions** **F** and **G**

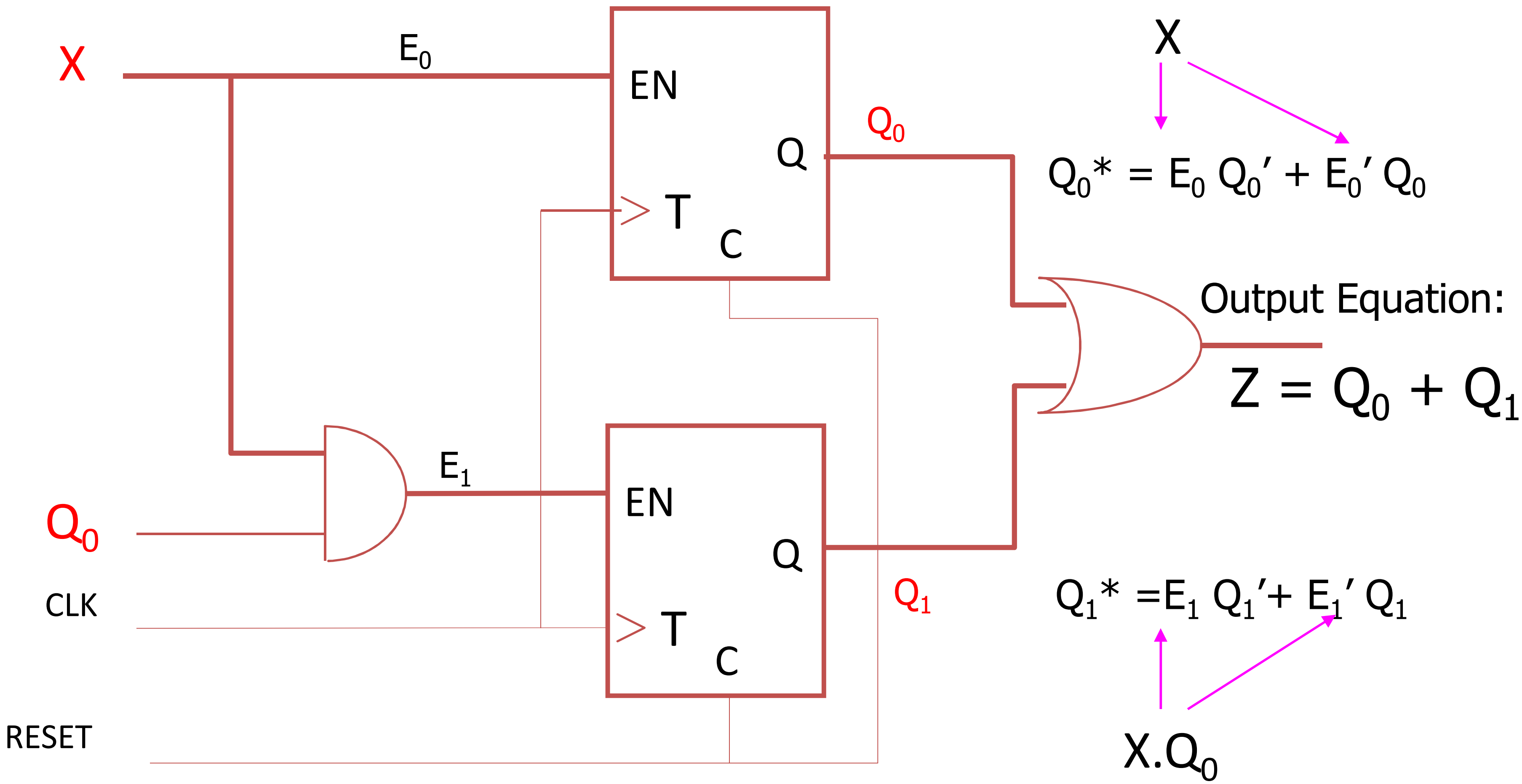
2. Use **F** and **G** to construct a **state table**

3. Draw a **state diagram** that represents the state table in graphical form

Detailed Analysis of State Machines

- Find flip-flop input **excitation equations**, D = f1 (state, inputs)
- Substitute excitation equations into flip-flop characteristic equations, giving **transition equations**, Q* = f2 (state, inputs)
- Construct a **transition table** from transition equations
- Find **output equations**, OUT = g (state) or g (state, inputs)
- Add outputs to to transition table to form **transition/output table**
- Name states in transition/output table, giving **state/output table**
- Draw a **state diagram** and **timing diagram** from state/output table

Example 1 - State Machine with T flip-flops



Characteristic Equation for T: $Q^* = EN.\, Q' + EN'\, Q$

Example 1 – Transition-State/Output Table

Transition Equations:

$Q_0^* = X\,Q_0' + X'\,Q_0$

$Q_1^* = X\,Q_0\,Q_1' + X'\,Q_1 + Q_0'\,Q_1$

Output Equation:

$Z = Q_0 + Q_1$

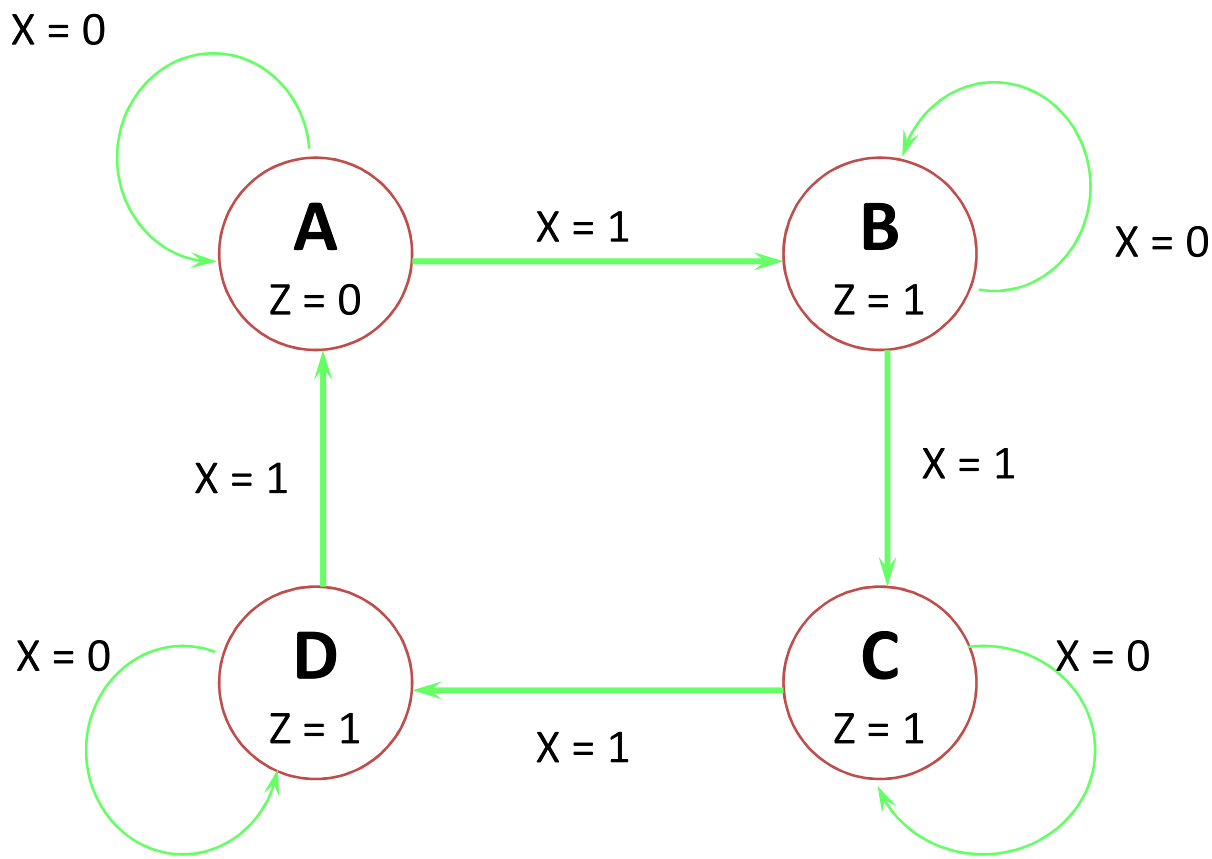
Q_1Q_0	X = 0	X = 1	Z
A = 0 0	0 0	0 1	0
B = 0 1	0 1	1 0	1
C = 1 0	1 0	1 1	1
D = 1 1	1 1	0 0	1
	$Q_1^*Q_0^*$		

Moore Machine

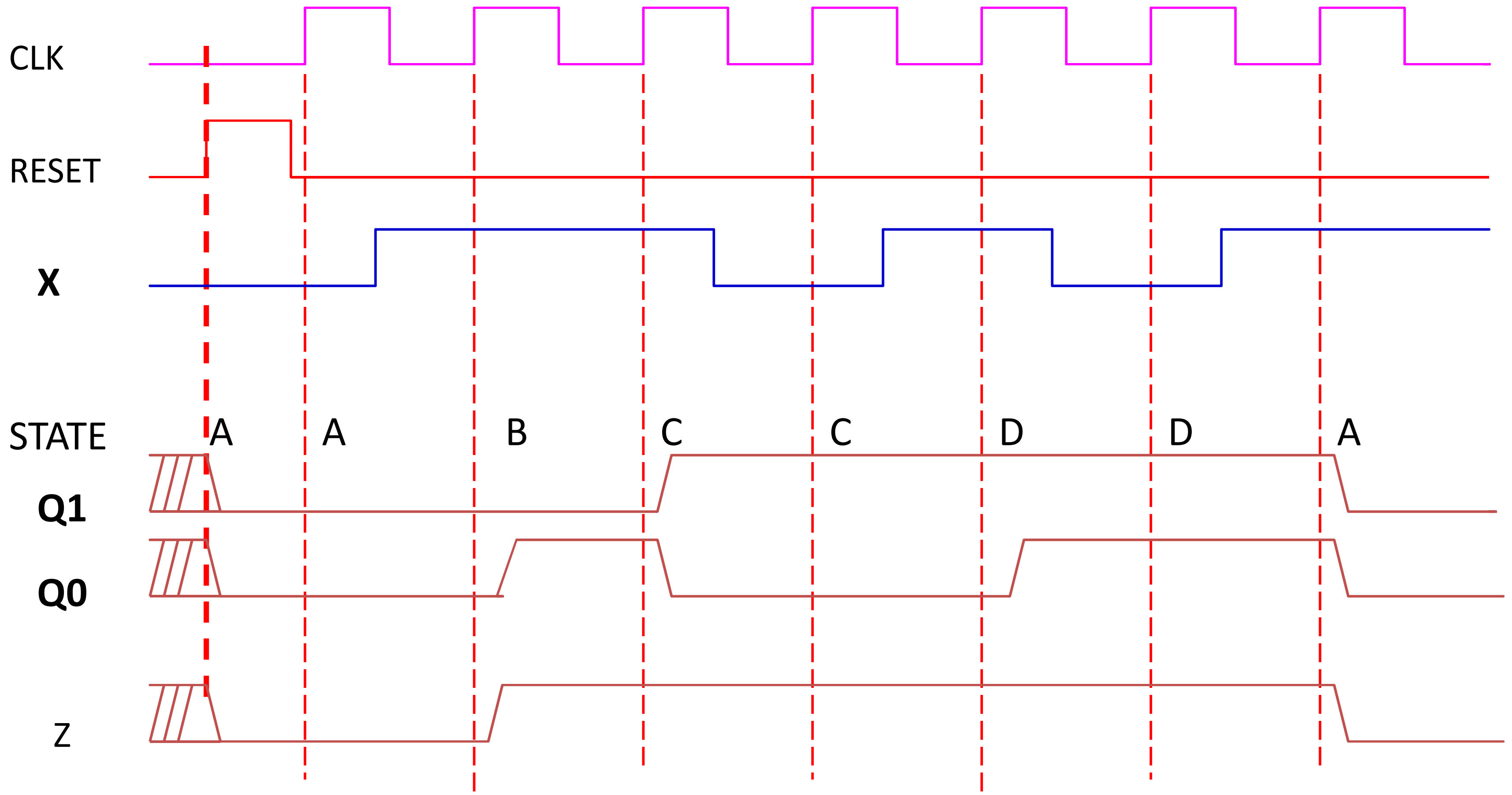
S	X = 0	X = 1	Z
A	A	B	0
B	B	C	1
C	C	D	1
D	D	A	1
	S^*		

Example 1 - State Diagram

	X		
S	0	1	Z
A	A	B	0
B	B	C	1
C	C	D	1
D	D	A	1
	S^*		

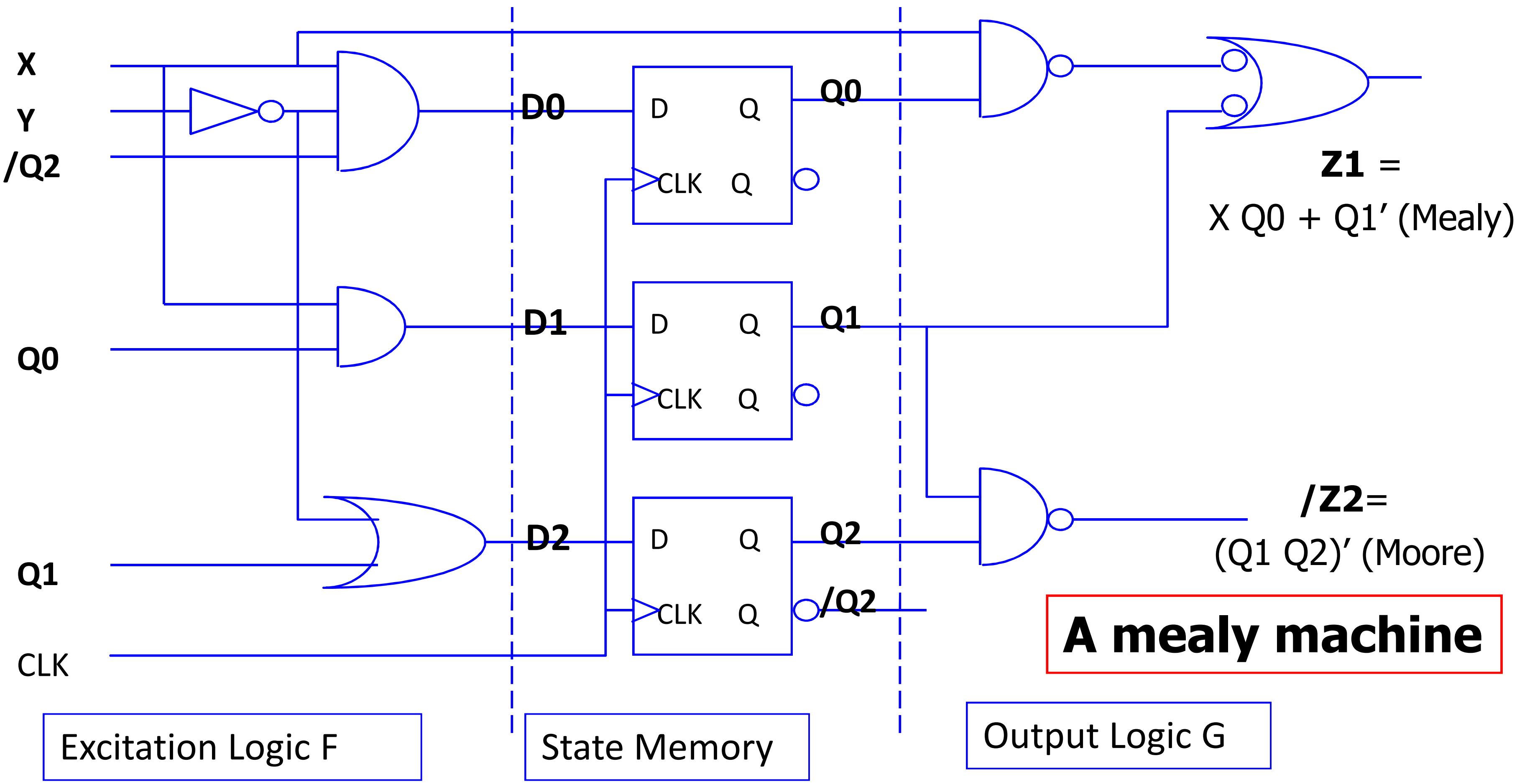


Example 1 - Timing diagram



Example 2 - State Machine with D Flip-flops

Excitation Equations: D0 = X Y′ Q2′; D1 = X Q0; D2 = Y′ +Q1



Example 2 - Equations

Characteristic Equation for D flip-flop: Q* = D

Excitation Equations:

D0 = X Y’ Q2’

D1 = X Q0

D2 = Y’ + Q1

⇒

Next State Equations:

Q0* = X Y’ Q2’

Q1* = X Q0

Q2* = Y’ + Q1

Output Equations:

Z1 = X Q0 + Q1’ (Mealy)

/Z2= (Q1 Q2)’ (Moore)

Example 2 - Transition / Output table

Q2 Q1 Q0	XY: 00	01	11	10
A = 0 0 0	100, 11	000, 11	000, 11	101, 11
B = 0 0 1	100, 11	000, 11	010, 11	111, 11
C = 0 1 0	100, 01	100, 01	100, 01	101, 01
D = 0 1 1	100, 01	100, 01	110, 11	111, 11
E = 1 0 0	100, 11	000, 11	000, 11	100, 11
F = 1 0 1	100, 11	000, 11	010, 11	110, 11
G = 1 1 0	100, 00	100, 00	100, 00	100, 00
H = 1 1 1	100, 00	100, 00	110, 10	110, 10
	Q2* Q1* Q0*, Z1 /Z2			

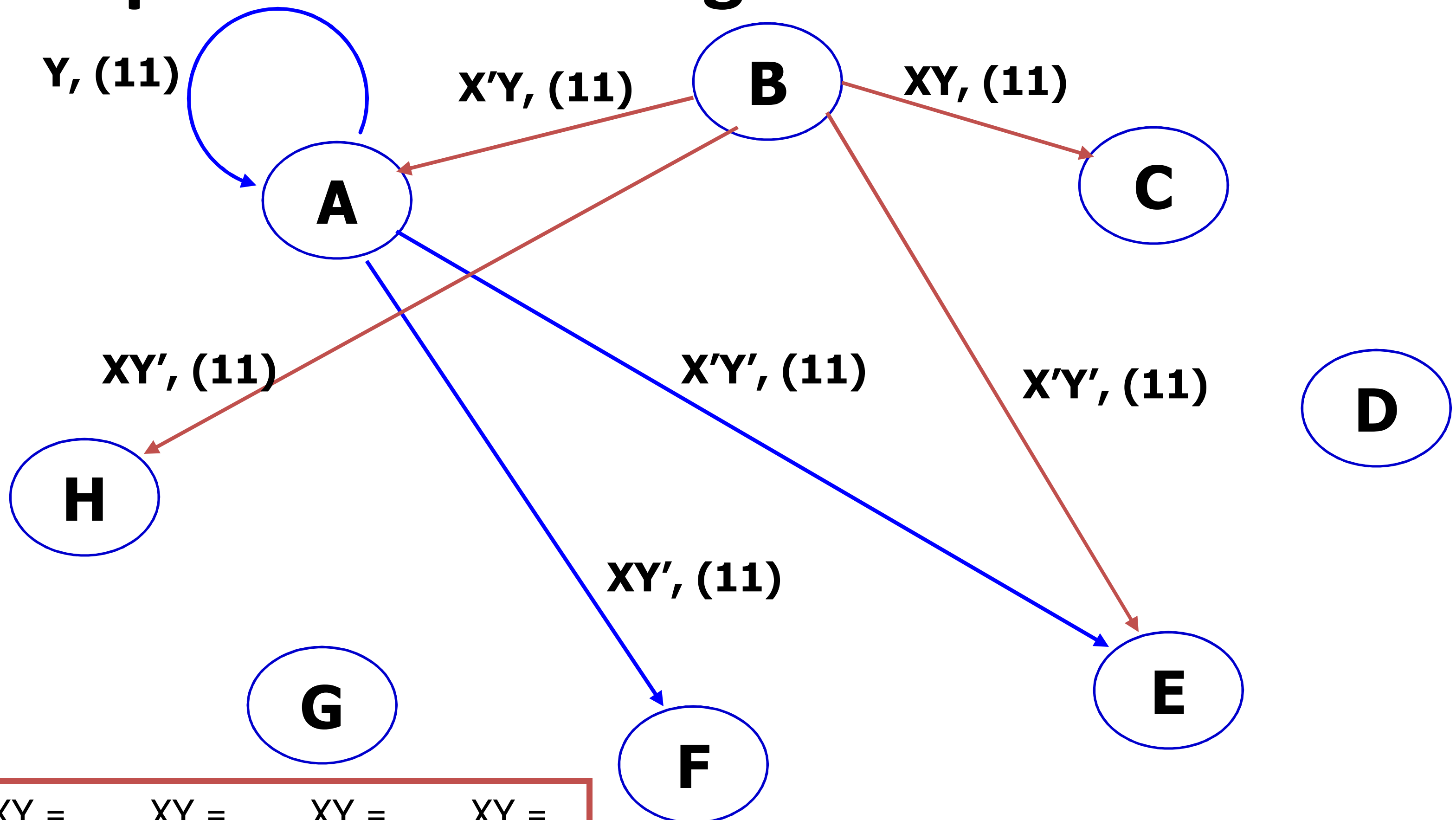
Q0* = X Y′ Q2′
Q1* = X Q0
Q2* = Y′ + Q1

Z1 = X Q0 + Q1′
/Z2= (Q1 Q2)′

Example 2 - State / Output table

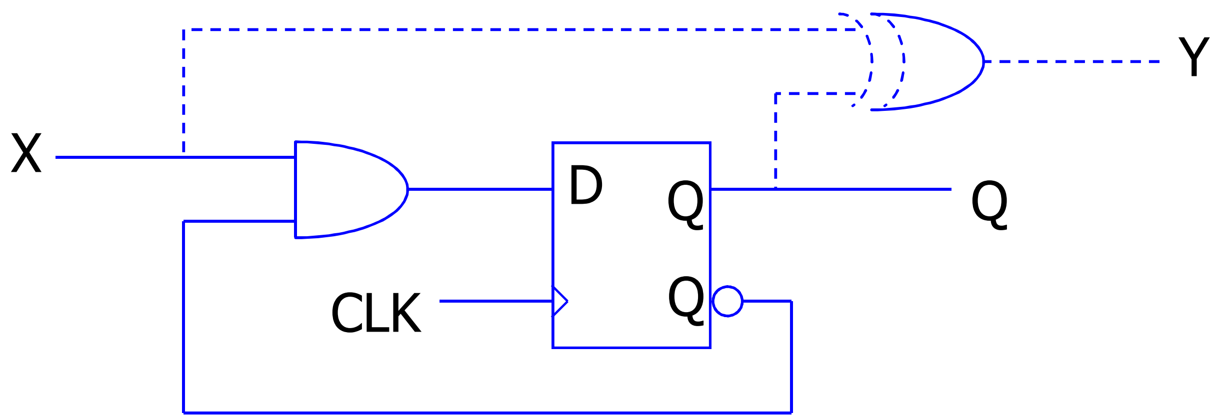
S	XY: 00	01	11	10
A	E, 11	A, 11	A, 11	F, 11
B	E, 11	A, 11	C, 11	H, 11
C	E, 01	E, 01	E, 01	F, 01
D	E, 01	E, 01	G, 11	H, 11
E	E, 11	A, 11	A, 11	E, 11
F	E, 11	A, 11	C, 11	G, 11
G	E, 00	E, 00	E, 00	E, 00
H	E, 00	E, 00	G, 10	G, 10
	S^*, Z1 /Z2			

Example 2 - State Diagram



S	XY = 00	XY = 01	XY = 11	XY = 10
A	E, 11	A, 11	A, 11	F, 11
B	E, 11	A, 11	C, 11	H, 11

Example 3 - Circuit and Equations



Moore

Excitation: $D = X \cdot Q' = Q^*$

Output: $Q = Q$

Mealy

Excitation: $D = X \cdot Q' = Q^*$

Output: $Y = X \oplus Q$

Example 3 - Tables

Excitation/Output Tables:

Moore

	X		
Q	***0***	***1***	***Z***
0	0	1	0
1	0	0	1
	Q^*		

Mealey

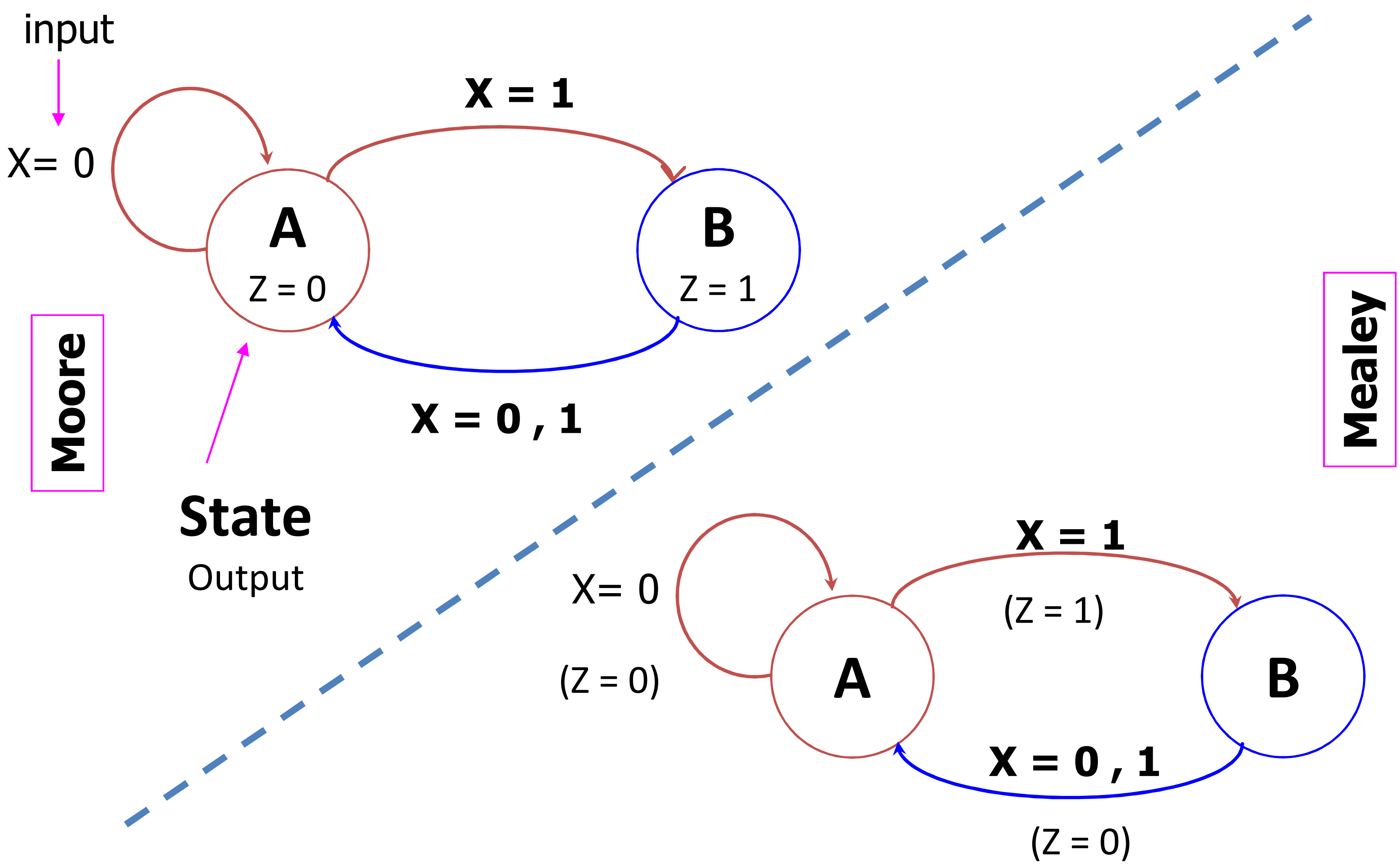
	X	
Q	***0***	***1***
0	0,0	1,1
1	0,1	0,0
	Q^*, Y	

State/Output Tables:

	X		
S	***0***	***1***	***Z***
A	A	B	0
B	A	A	1
	Q^*		

	X	
S	***0***	***1***
A	A, 0	B, 1
B	A, 1	A, 0
	S^*, Y	

Example 3 - State Diagrams



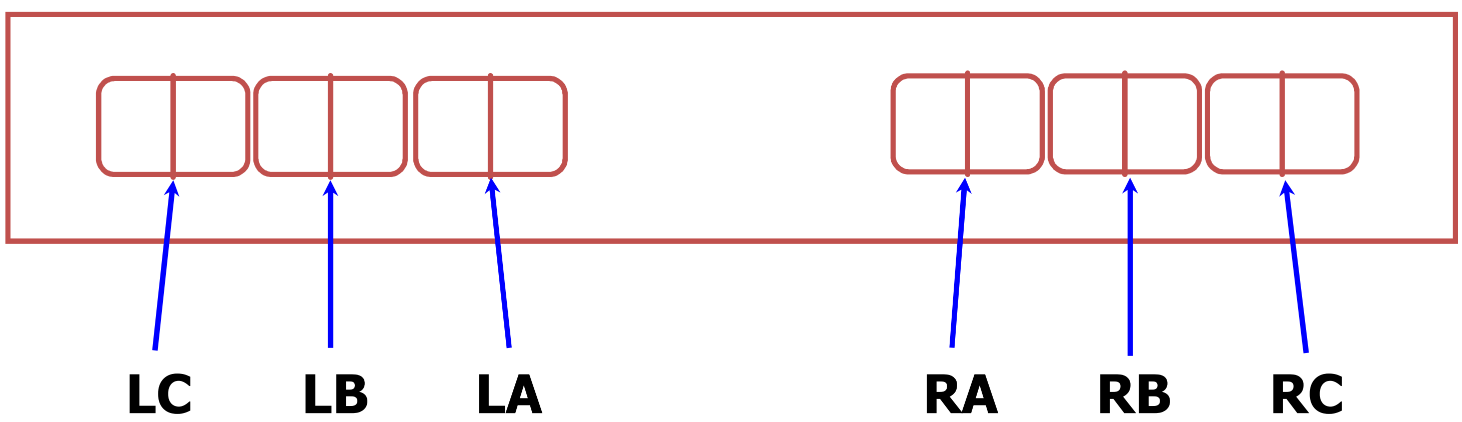
Synchronous Design with State Machines : State Diagram Design

- **State Table** covers **all** input combinations and states
- **State Diagram** has arcs with input combinations or transition equations
    - **More graphical** than state table design
    - Often simpler, but error prone
    - No guarantee of all input combinations
    - Possibly ambiguous - possibly no next state or more than one next state for some input combinations

Example- T-bird Tail Lights

- **3 inputs - LEFT, RIGHT, HAZ**

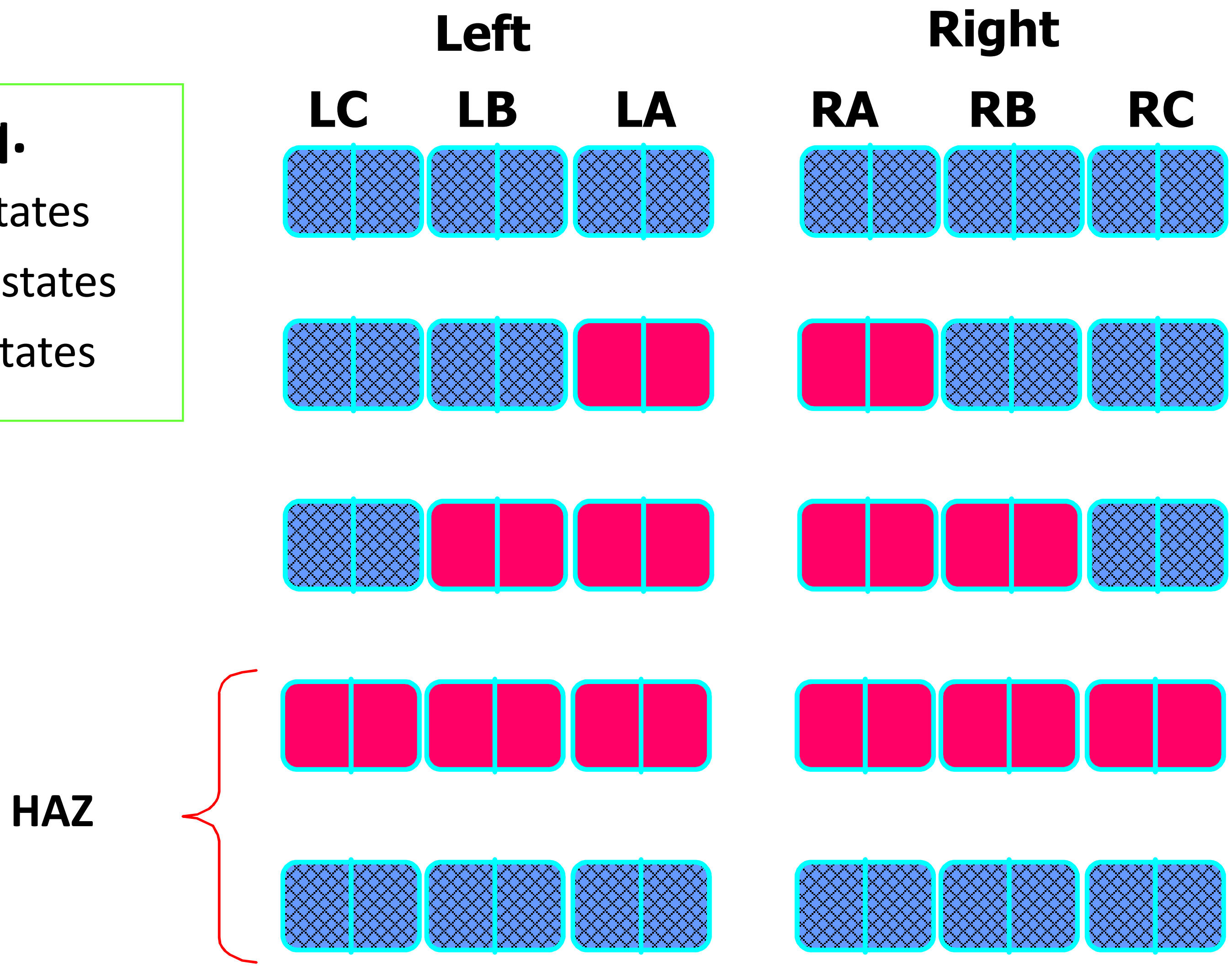
Layout of tail lights



Example- T-bird Tail Lights

Tail Light seq.

- Left = 4 states
- Right = 4 states
- HAZ = 2 states



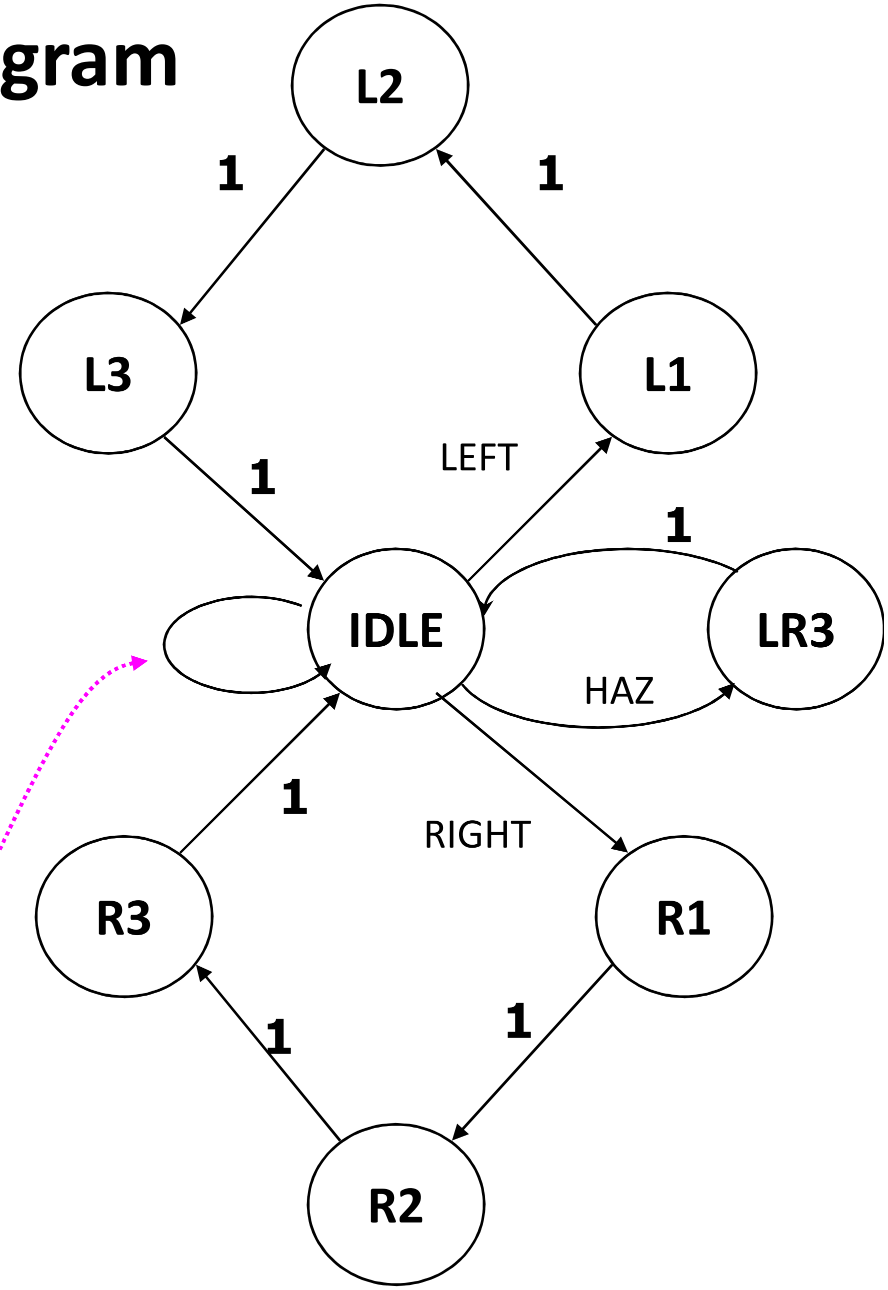
Example- First State Diagram

1. Moore Machine design

2. LEFT + RIGHT + HAZ starts sequence, continues unconditionally

3. If multiple inputs TRUE?→ multiple next states! PROBLEM!

4. Transitions need to be **mutually exclusive** and **all inclusive**

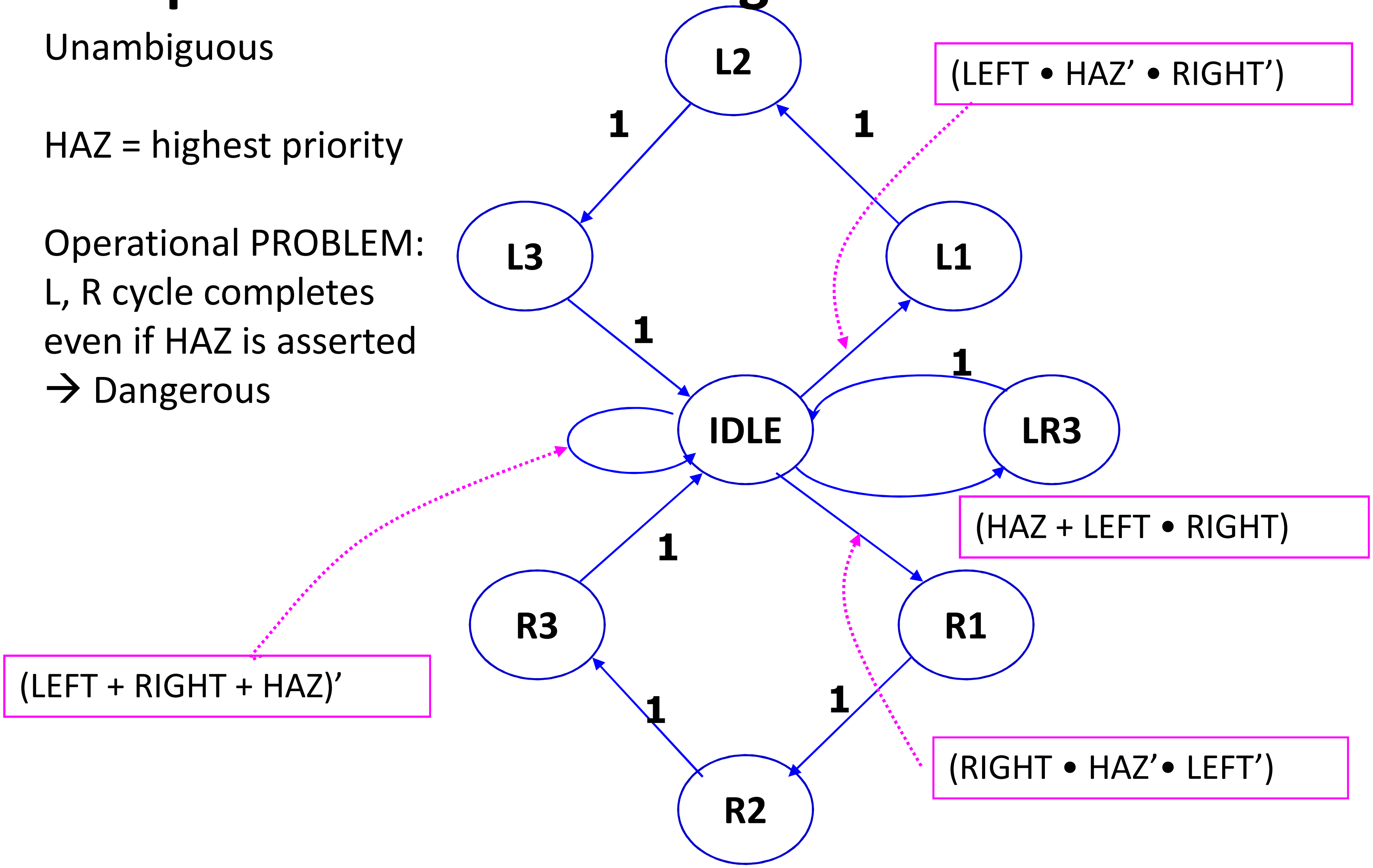


Example- Output Table

State	LC	LB	LA	RA	RB	RC
IDLE	0	0	0	0	0	0
L1	0	0	1	0	0	0
L2	0	1	1	0	0	0
L3	1	1	1	0	0	0
R1	0	0	0	1	0	0
R2	0	0	0	1	1	0
R3	0	0	0	1	1	1
LR3	1	1	1	1	1	1

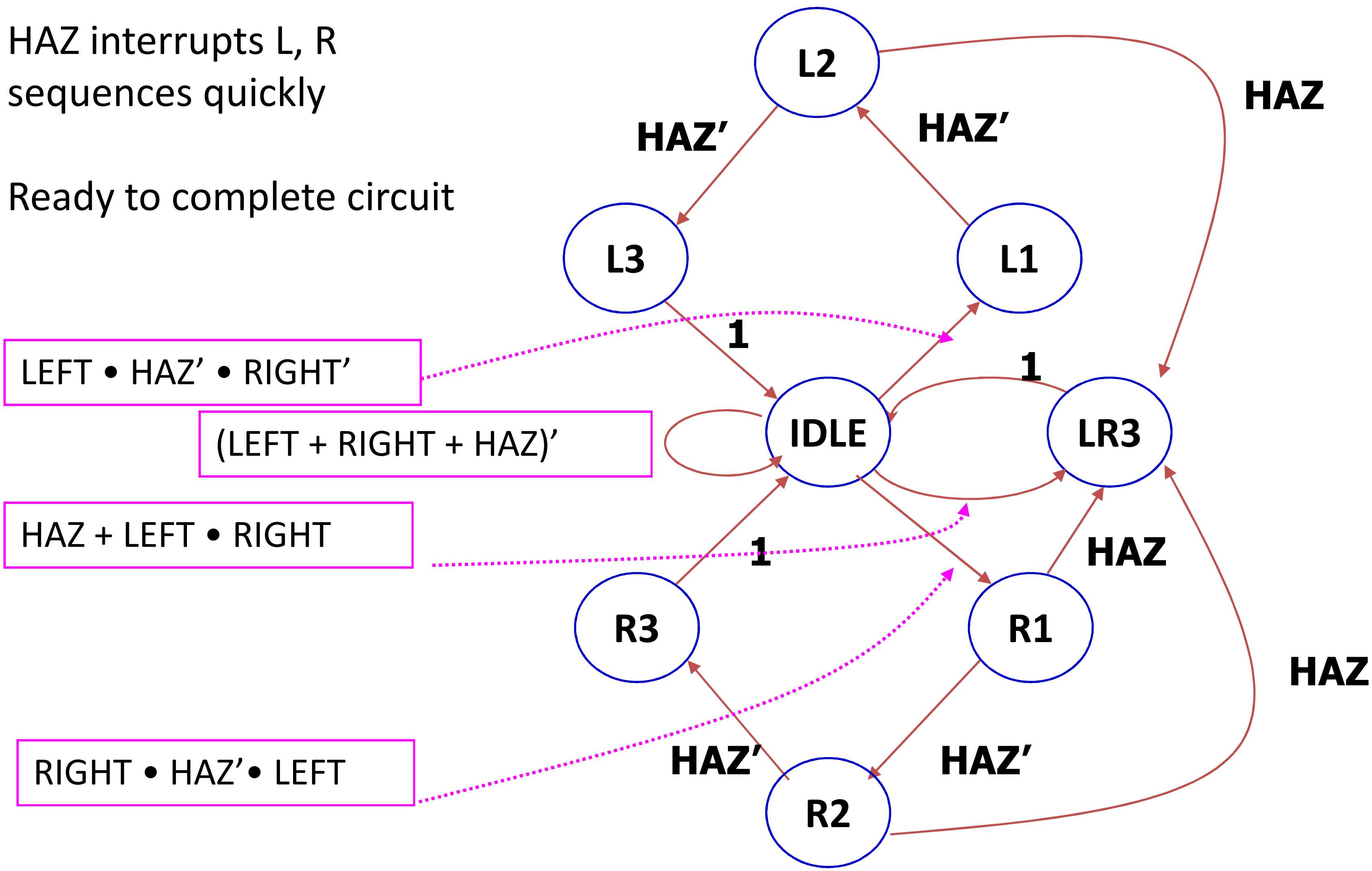
Example- Second State Diagram

- Unambiguous
- HAZ = highest priority
- Operational PROBLEM: L, R cycle completes even if HAZ is asserted → Dangerous



Example- Third State Diagram

- HAZ interrupts L, R sequences quickly
- Ready to complete circuit



Example- State Assignment

State Assignment:

- Initially all zeros
- **Q2** determines Left vs. Right turn sequence
- **Q1 Q0** count gray-code sequence to minimize state variable transitions

Example- Transition List

Alternative to transition table for state diagram design method

One row per transition

S	Q2 Q1 Q0	Transition Expr	S*	Q2*Q1*Q0*
IDLE	0 0 0	(LEFT+RIGHT+HAZ)’	IDLE	0 0 0
IDLE	0 0 0	LEFT+HAZ’.RIGHT’	L1	0 0 1
IDLE	0 0 0	HAZ+LEFT.RIGHT	LR3	1 0 0
IDLE	0 0 0	RIGHT.HAZ’.LEFT’	R1	1 0 1
L1	0 0 1	HAZ’	L2	0 1 1
L1	0 0 1	HAZ’	LR3	1 0 0
L2	0 1 1	HAZ’	L3	0 1 0
L2	0 1 1	HAZ	LR3	1 0 0
L3	0 1 0	1	IDLE	0 0 0
R1	1 0 1	HAZ’	R2	1 1 1
R1	1 0 1	HAZ	LR3	1 0 0
R2	1 1 1	HAZ’	R3	1 1 0
R2	1 1 1	HAZ	LR3	1 0 0
R3	1 1 0	1	IDLE	0 0 0
LR3	1 0 0	1	IDLE	0 0 0

Example- Next State and Output Generation

$Q2^* = Q2'.Q1'.Q0'.(HAZ+RIGHT) + Q2'.Q0.HAZ+Q2.Q0$

$Q1^* = Q0.HAZ'$

$Q0^* = Q2.Q1'.HAZ'.(LEFT \oplus RIGHT) + Q1'.Q0.HAZ'$

Example- Output Table

	State	LC	LB	LA	RA	RB	RC
000	IDLE	0	0	0	0	0	0
001	L1	0	0	1	0	0	0
011	L2	0	1	1	0	0	0
010	L3	1	1	1	0	0	0
101	R1	0	0	0	1	0	0
111	R2	0	0	0	1	1	0
110	R3	0	0	0	1	1	1
100	LR3	1	1	1	1	1	1

$LA = Q2'.Q0 + Q2'.Q1 + Q2.Q1'.Q0'$

$LB = Q2'.Q1 + Q2.Q1'.Q0'$

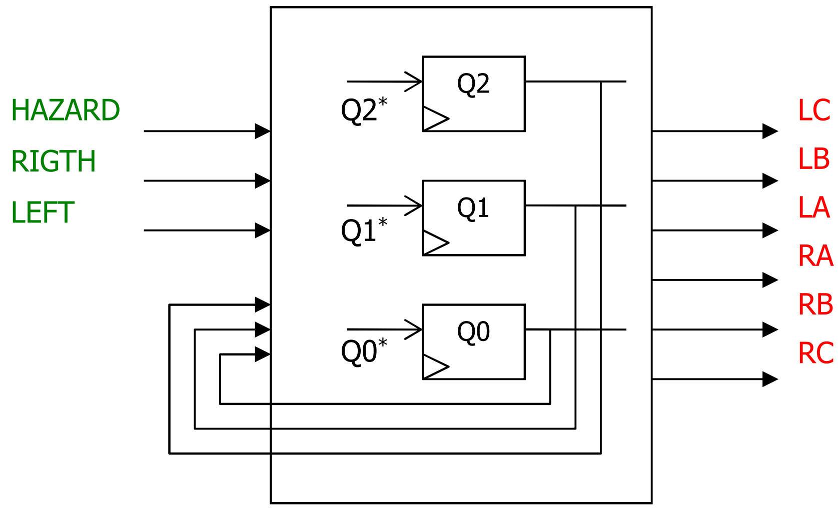
$LC = Q2'.Q1.Q0' + Q2.Q1'.Q0'$

$RA = Q2$

$RB = Q2.Q0' + Q2.Q1$

$RC = Q2.Q0'$

Example- Circuit Block Diagram



Example- Circuit Diagram