Faculty of Engineering

CSE115: Digital Design

Lecture 19:
XORs and Parity Circuits

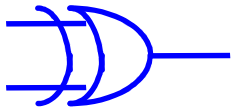
Suggested Reading

- Section 5.8

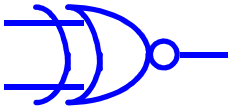
2-input XOR Gates

Like an OR gate, but **excludes** the case where both inputs are 1.

X	Y	XOR	XNOR
0	0	**0**	**1**
0	1	**1**	**0**
1	0	**1**	**0**
1	1	**0**	**1**

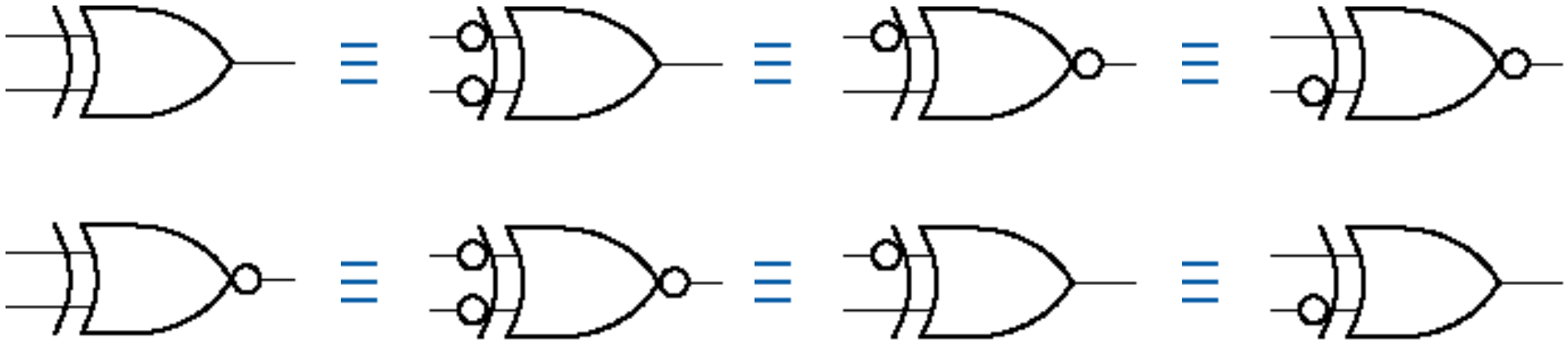


$$X \oplus Y = X' \cdot Y + X \cdot Y'$$



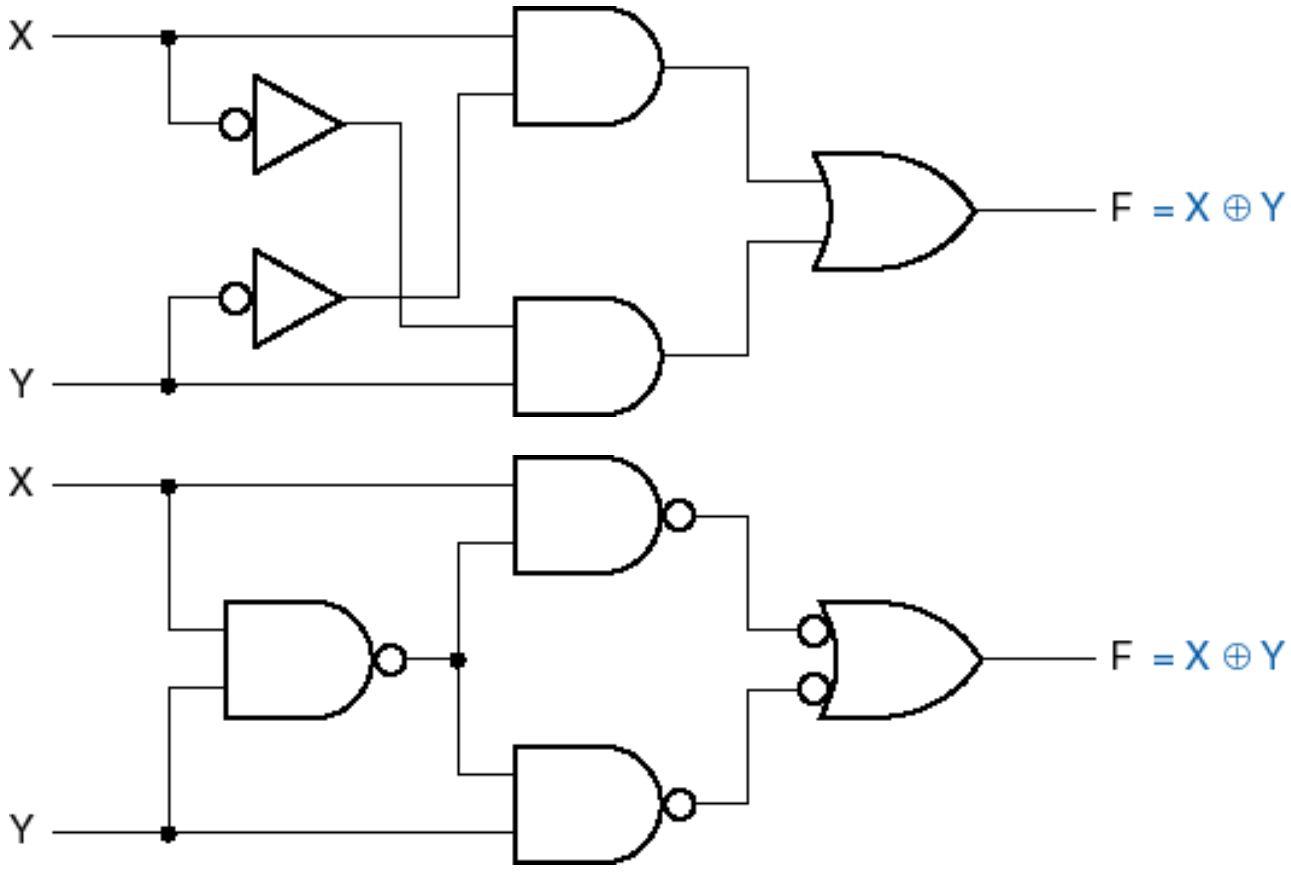
$$(X \oplus Y)' = X \cdot Y + X' \cdot Y'$$

XOR and XNOR Symbols



Gate-level XOR Circuits

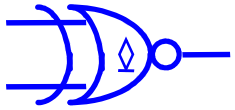
No direct realization with just a few transistors.



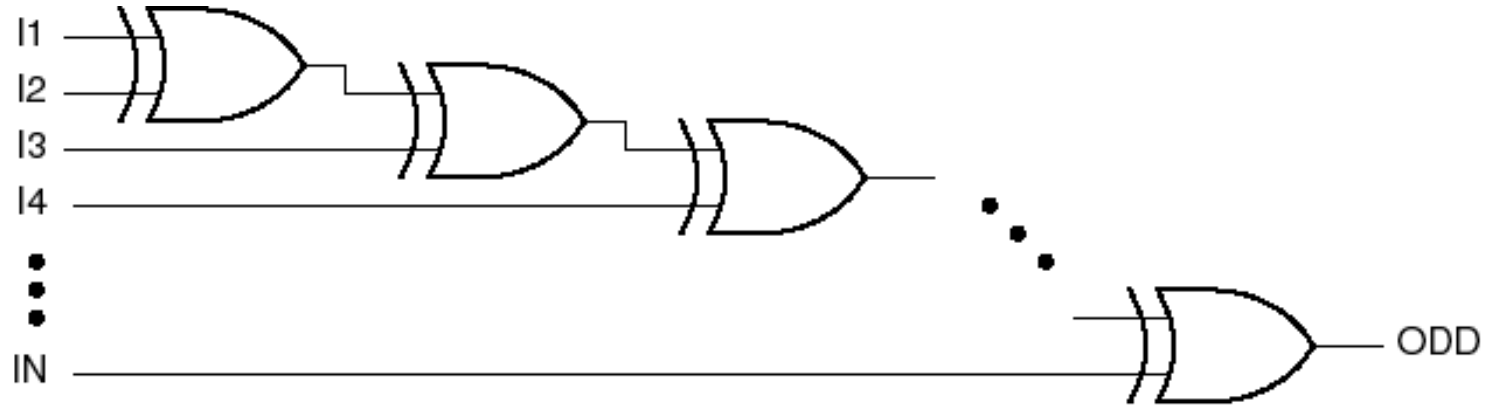
SSI XOR

74x86: 4 XOR gates

74x266: 4 XNOR gates



Parity Circuit: Daisy Chain



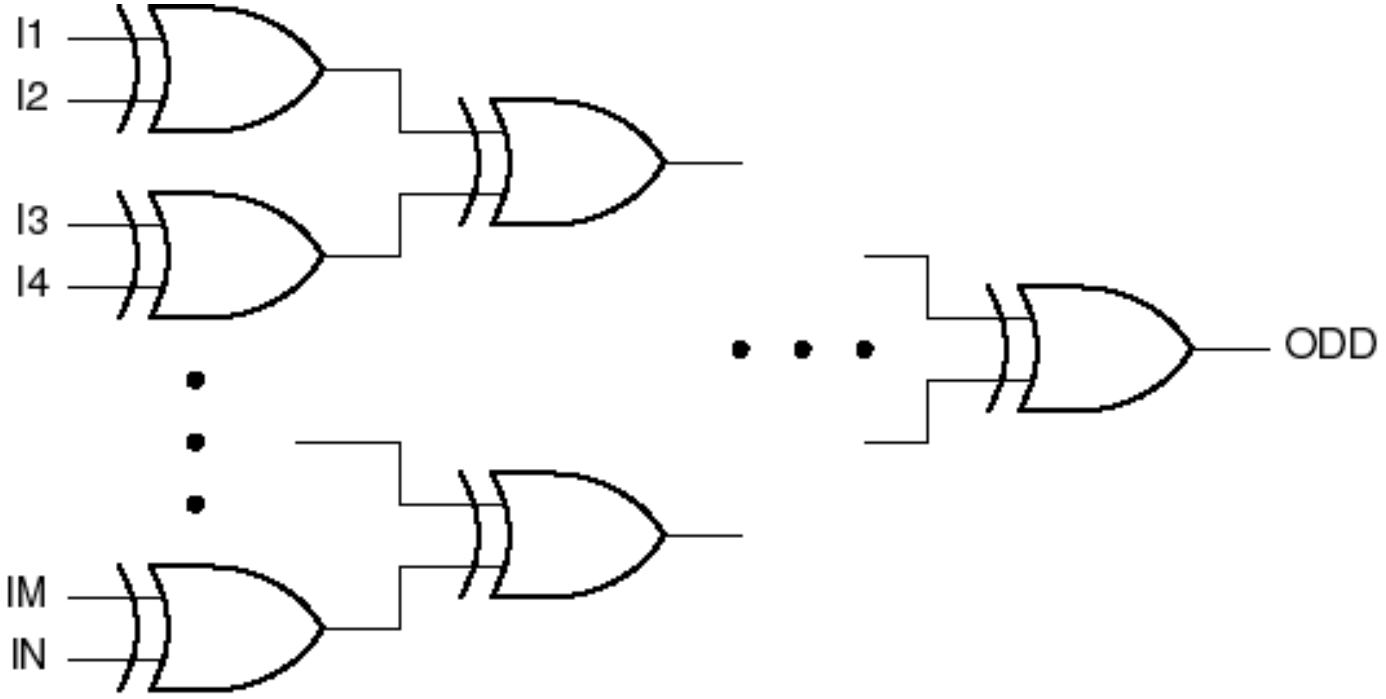
Odd Parity Circuit: The output is 1 if odd number of inputs are 1

Even Parity Circuit: The output is 1 if even number of inputs are 1

- Used to generate and check parity bits in computer systems.
- Detects any single-bit error

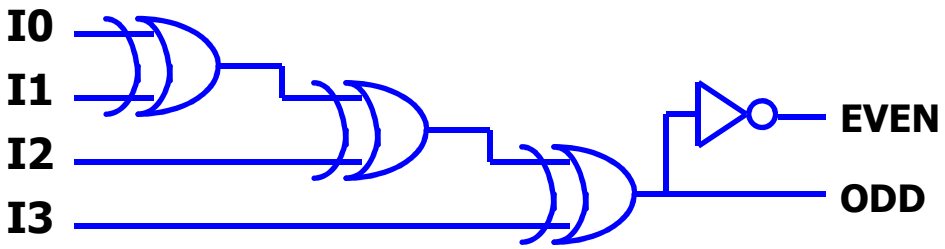
Parity Tree

Faster with balanced tree structure

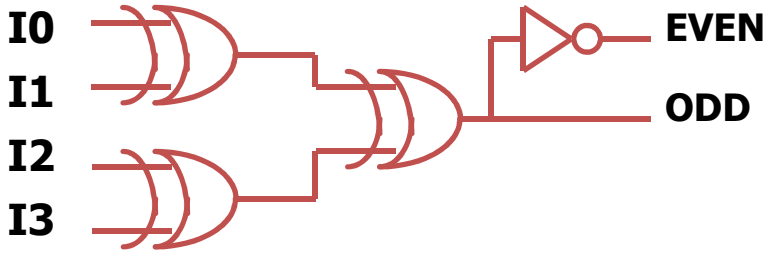


XOR Example:

Daisy-Chain Structure



Tree structure



Input: 1101

Even Parity output: **0**

Odd Parity output: **1**