Faculty of Engineering

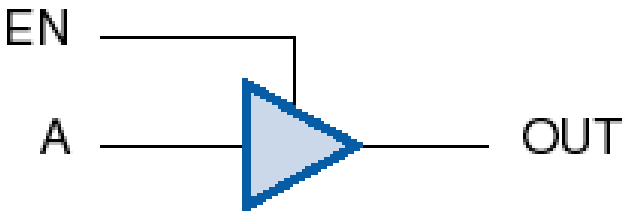
CSE115: Digital Design

Lecture 17:
Three State Logic

Suggested Reading

- Sections 5.6

Three-State Buffers



Output = LOW, HIGH, or Hi-Z.

Hi-Z: The output is floating (High Impedance) when the enable input is deasserted →

The input is isolated from the output

EN	A	OUT
L	L	Hi-Z
L	H	Hi-Z
H	L	L
H	H	H

Application:

- Can tie multiple outputs together, if at most one at a time is driven.
- Controlling the access of **a single line/bus** by multiple devices.

Different Types

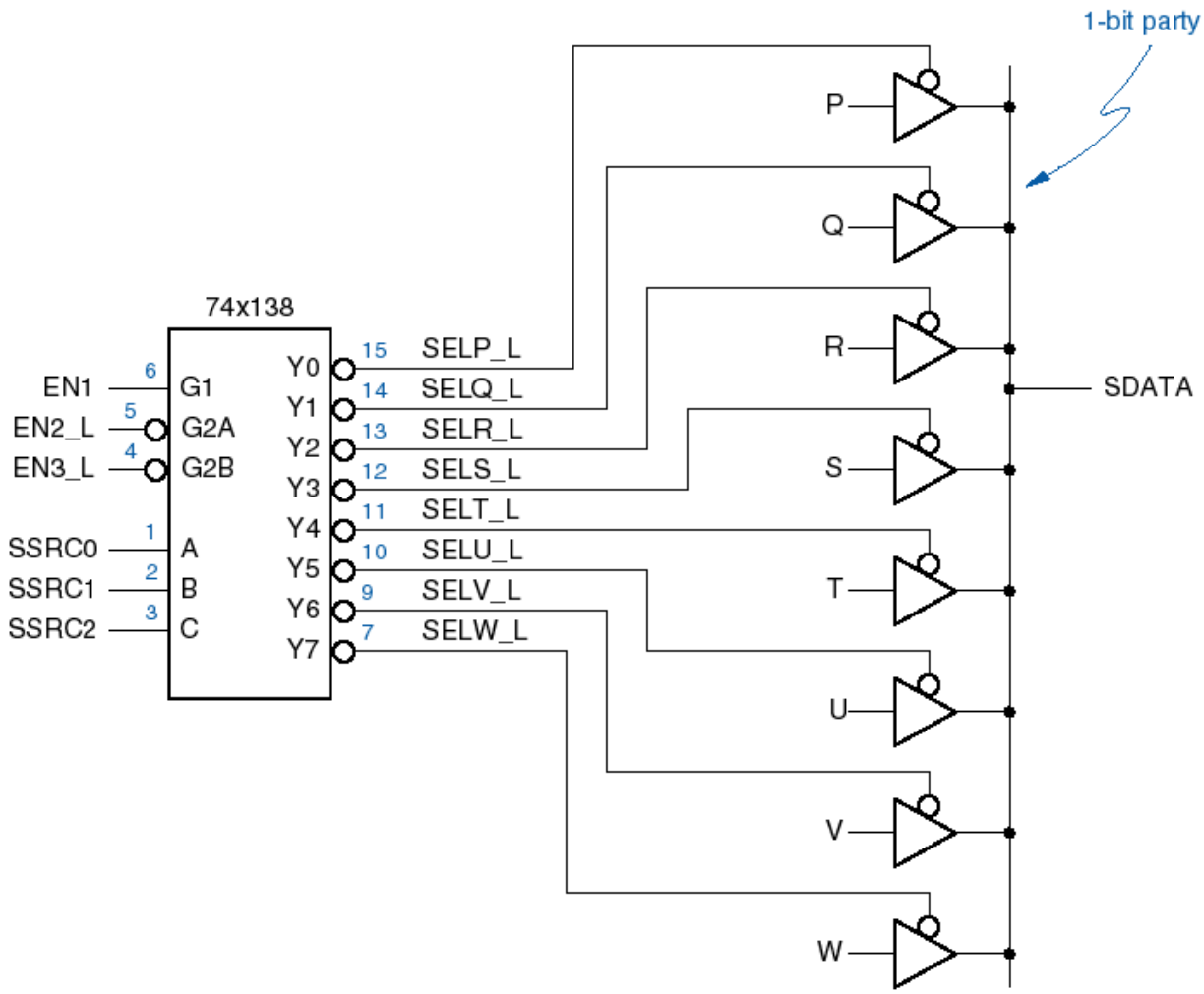
Active High Enable Active Low Enable

Buffers

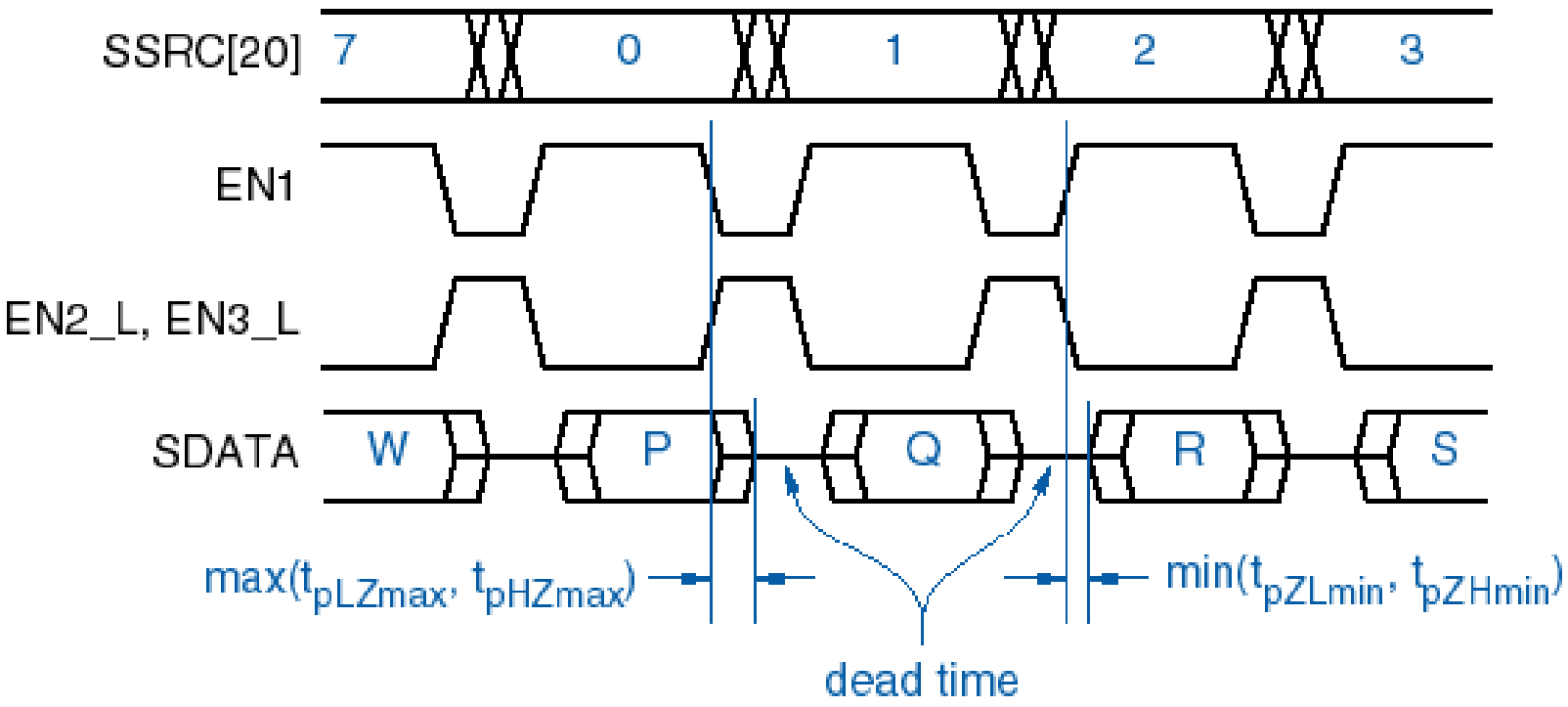
Active High Enable Active Low Enable

Inverters

8 Data Sources Sharing One Line



Timing Considerations



SSI/MSI Three-State Buffers

74x125: 4 independent buffers, Active Low enable

74x126: 4 independent buffers, Active High enable

74x540: 8 inverters with a common enable input

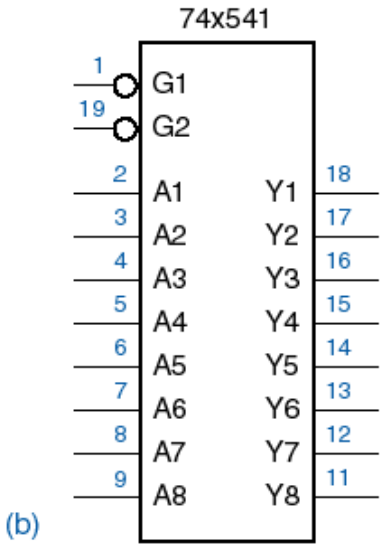
74x541: 8 buffers with a common enable input

74x240: 2 sets of 4 inverters with a common enable for each set

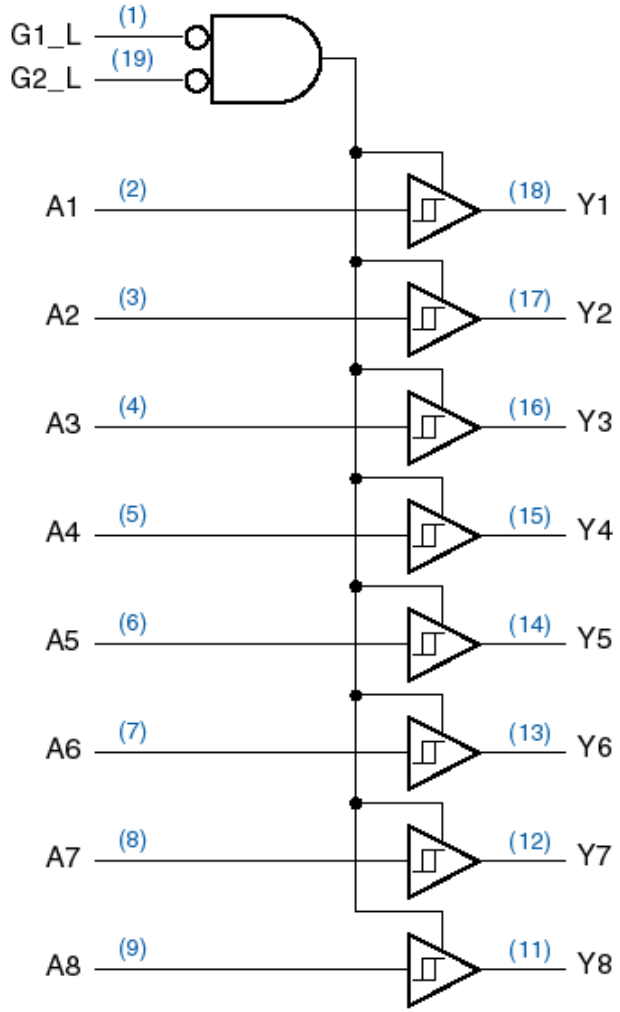
74x241: 2 sets of 4 buffers with a common enable for each set

74x245: *Octal three-state transceiver*
8 pairs of buffers connected in opposite directions

Three-State Drivers

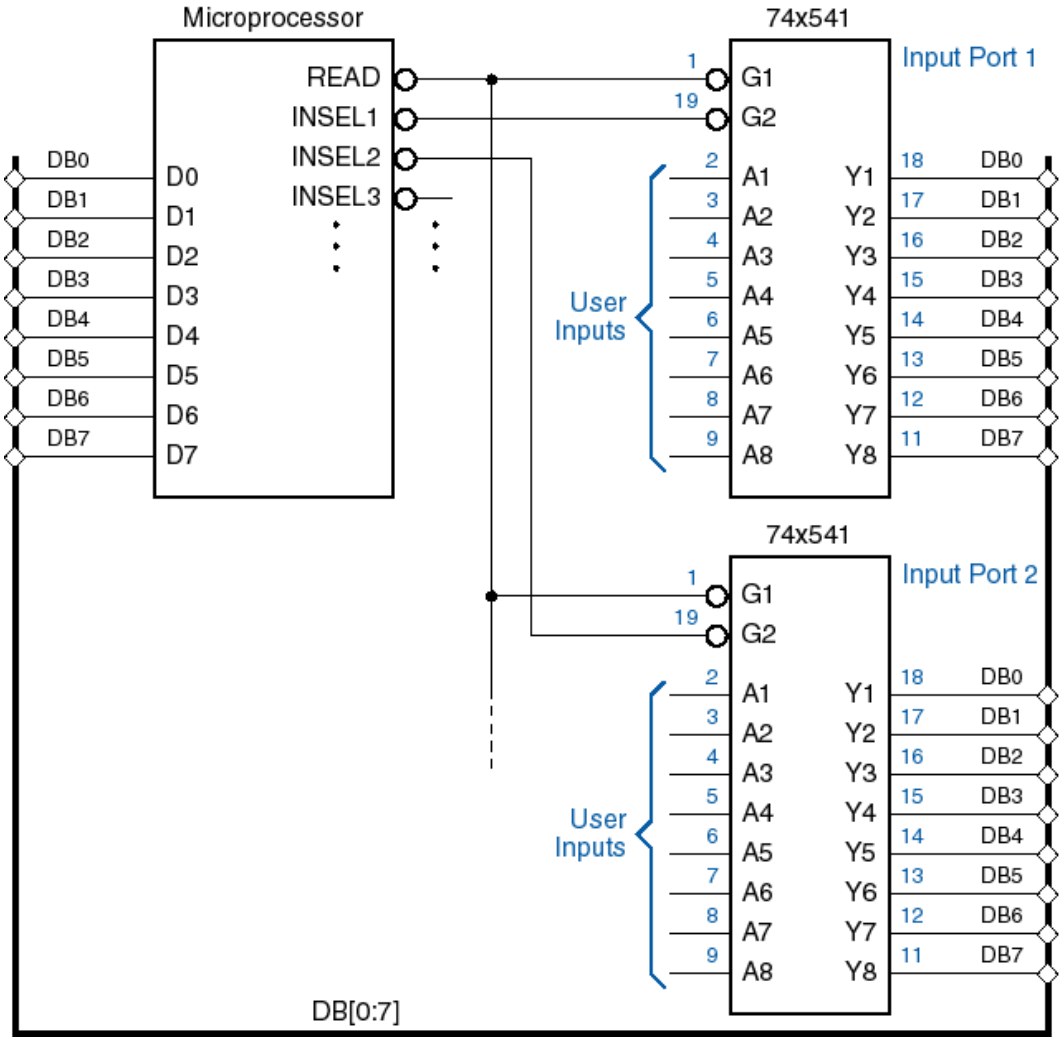


(b)

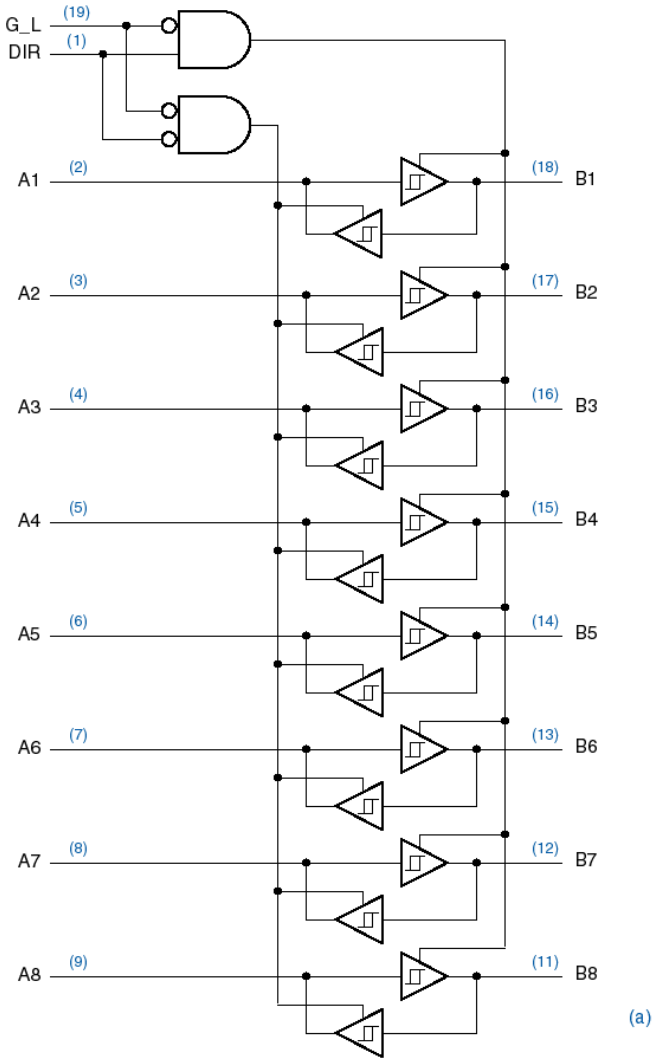


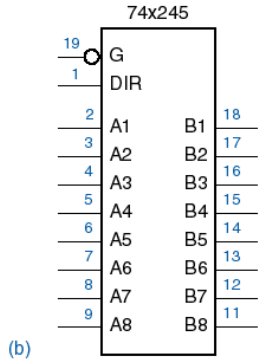
(a)

Driver Application



Three-State Transceiver





Transceiver Application