Faculty of Engineering

CSE115: Digital Design

Lecture 14:
Programmable Logic Arrays

Suggested Reading

- Sections 5.3

Programmable Logic Arrays (PLAs)

Any combinational logic function can be realized as a sum of products.

Idea: Build a large AND-OR array with lots of inputs and product terms, and programmable connections.

- ***n*** inputs

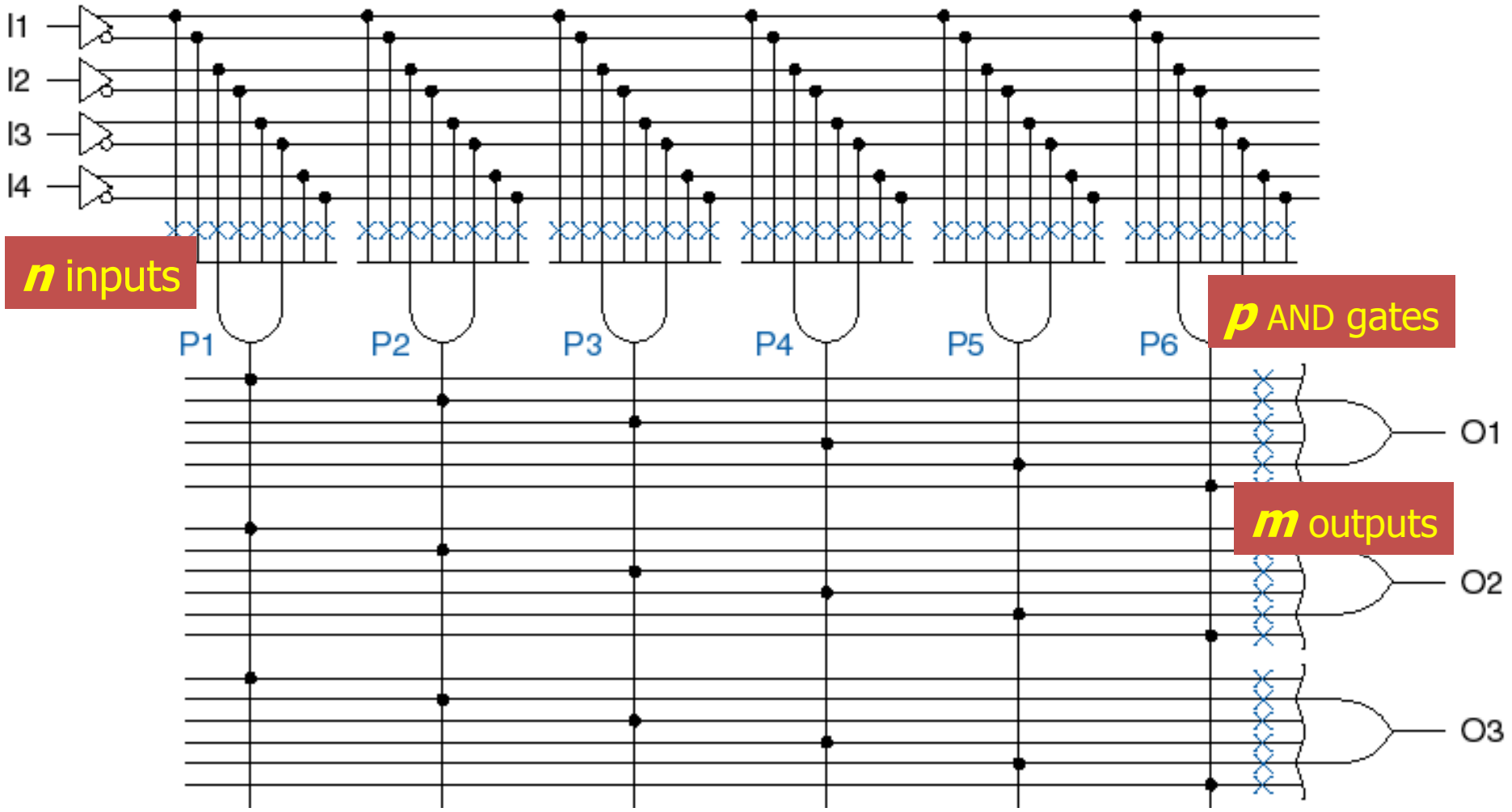
  AND gates have 2*n* inputs -true and complement of each variable

- ***m*** outputs, driven by large OR gates

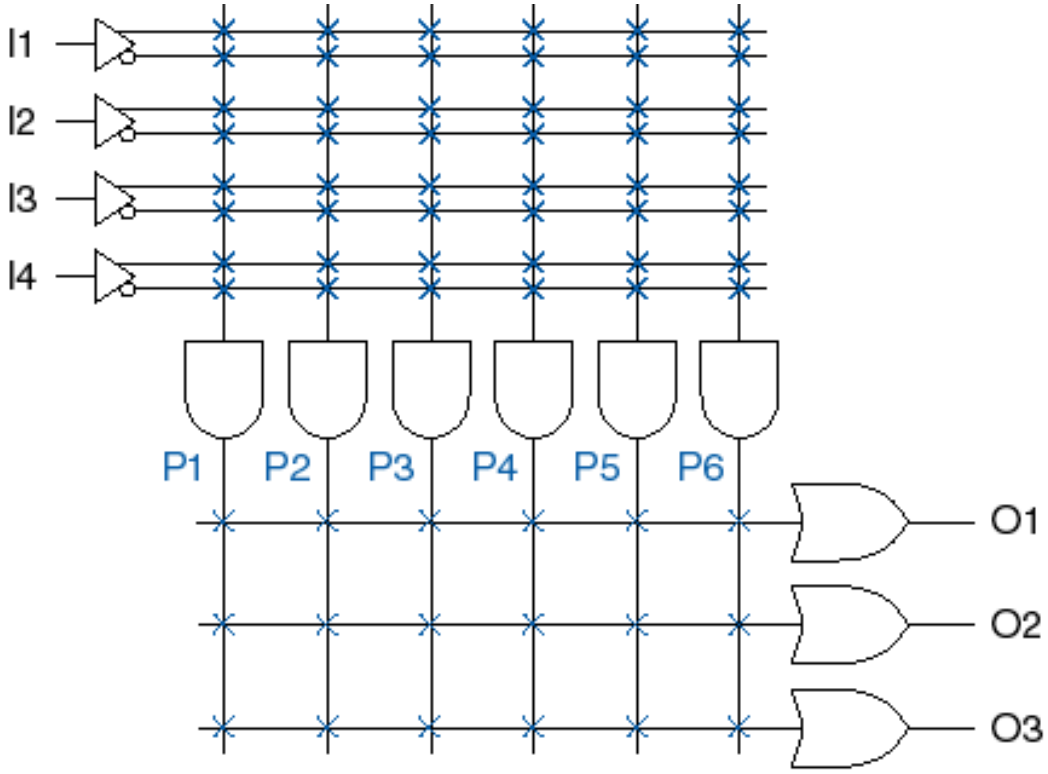
  Each AND gate is programmably connected to each output's OR gate

- ***p*** AND gates ($p << 2^n$)

Example: 4x3 PLA, 6 Product Terms

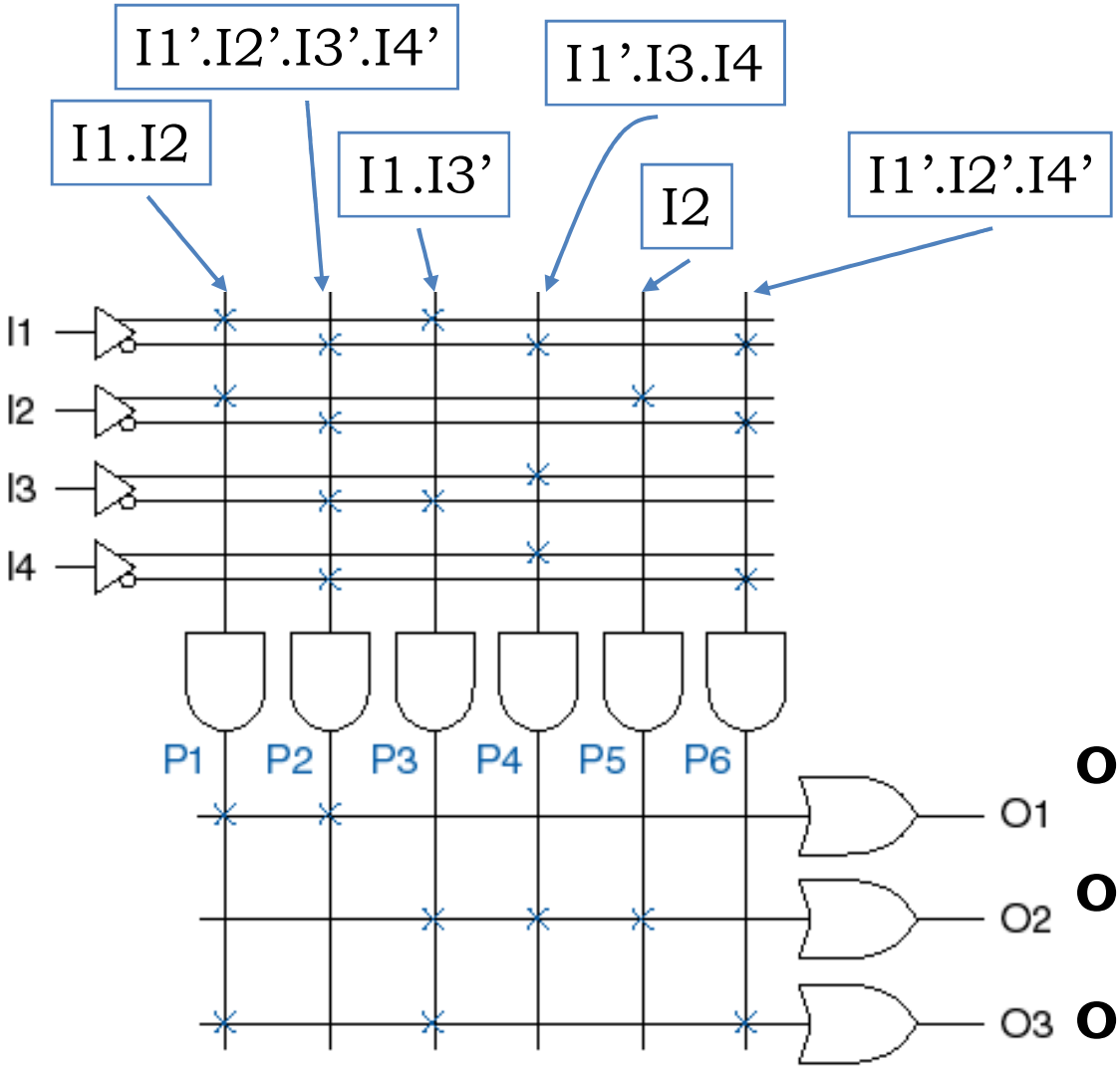


Compact Representation



Actually, closer to physical layout ('wired logic')

Some Product Terms

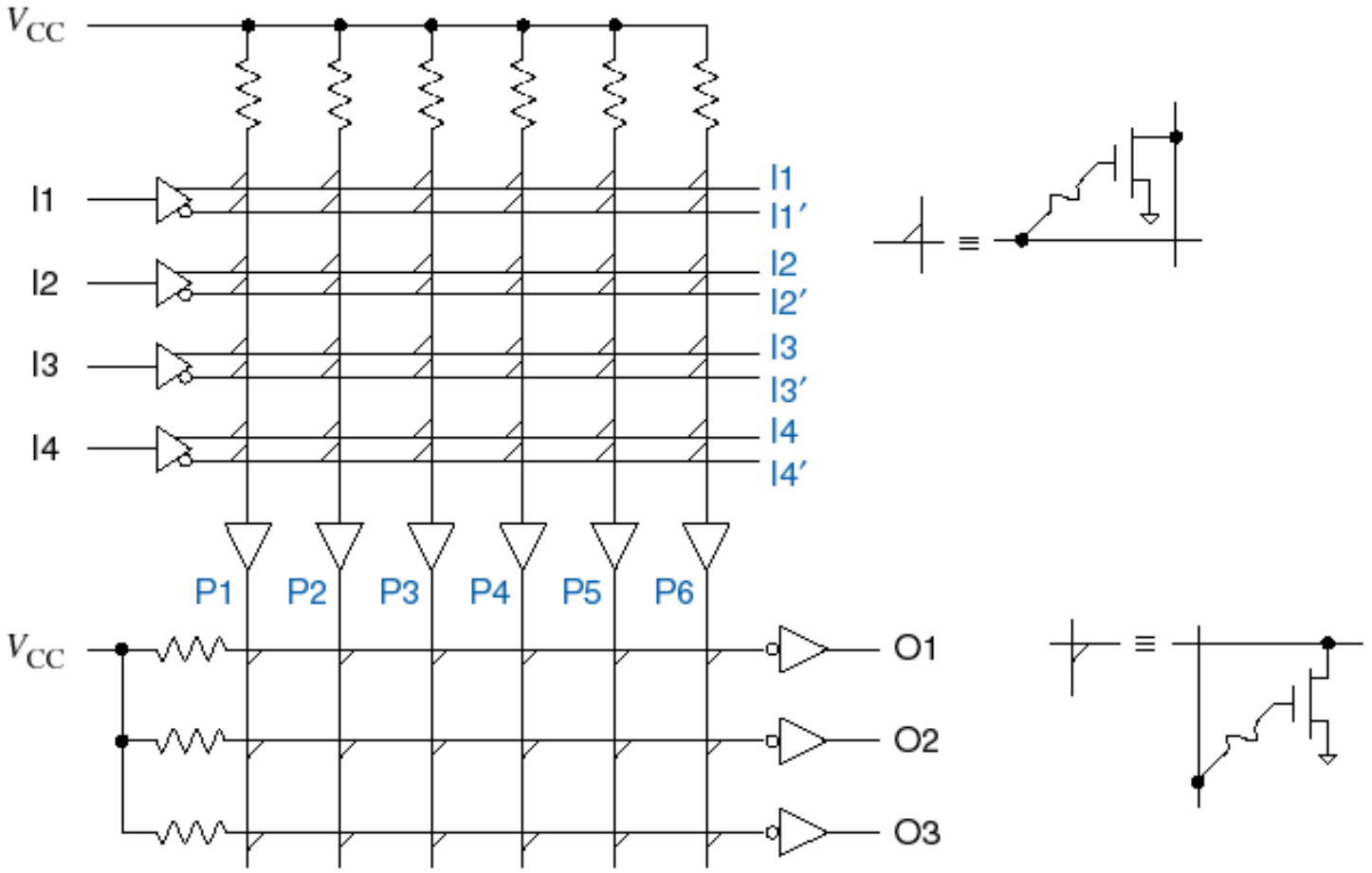


O1 = I1.I2 + I1'.I2'.I3'.I4'

O2 = I1.I3' + I1'.I3.I4 + I2

O3 = I1.I2 + I1.I3' + I1'.I2'.I4'

PLA Electrical Design



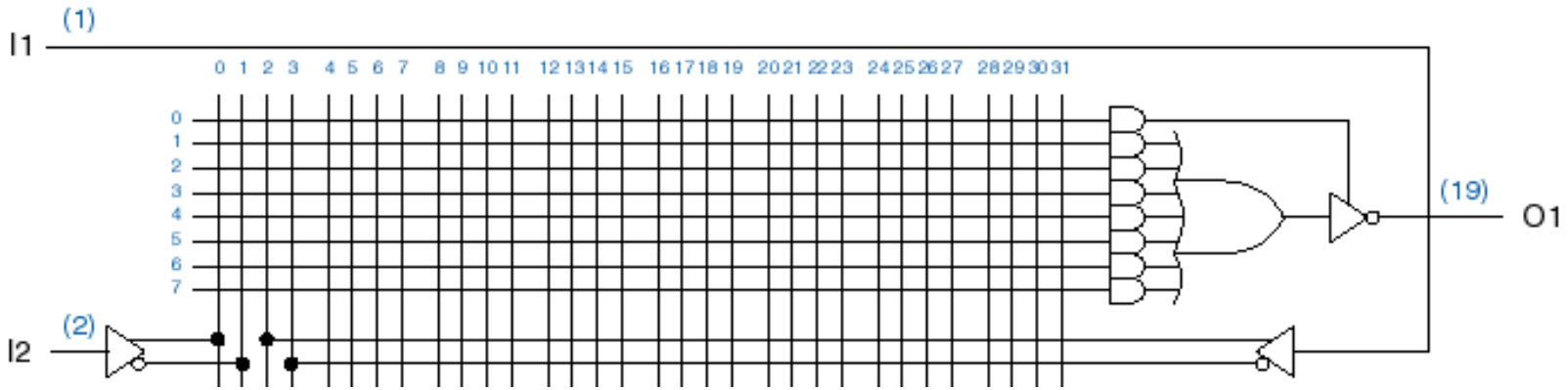
Programmable Array Logic (PALs)

How beneficial is product sharing?

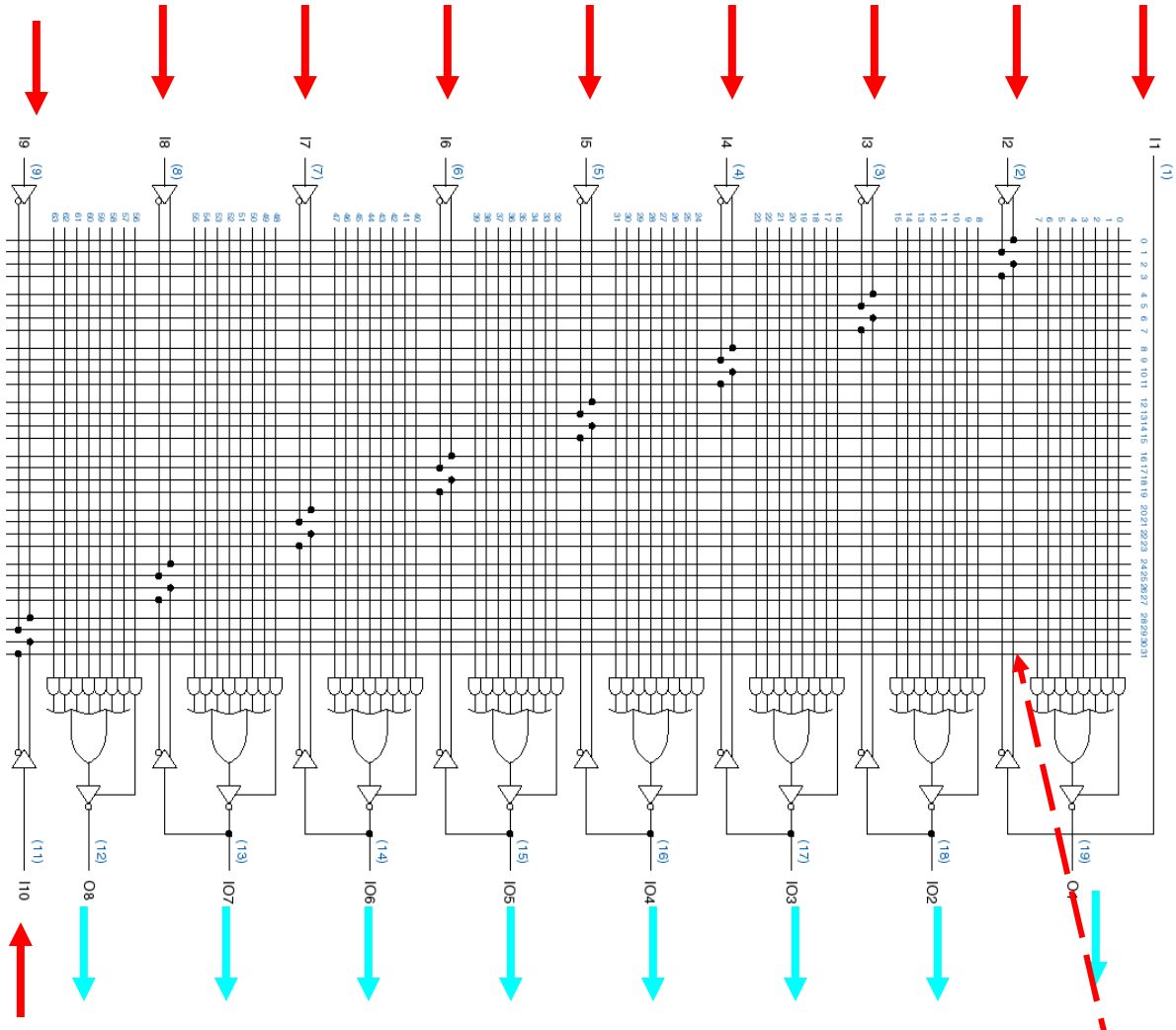
Not enough to justify the extra **AND** array

PALs → fixed **OR** array

Example: PAL16L8



10 primary **inputs**



8 **outputs**

6 outputs available as inputs

7 ANDs per output and
1 AND for 3-state enable