Faculty of Engineering

CSE115: Digital Design

Lecture 13:
Combinational Logic Design Practices

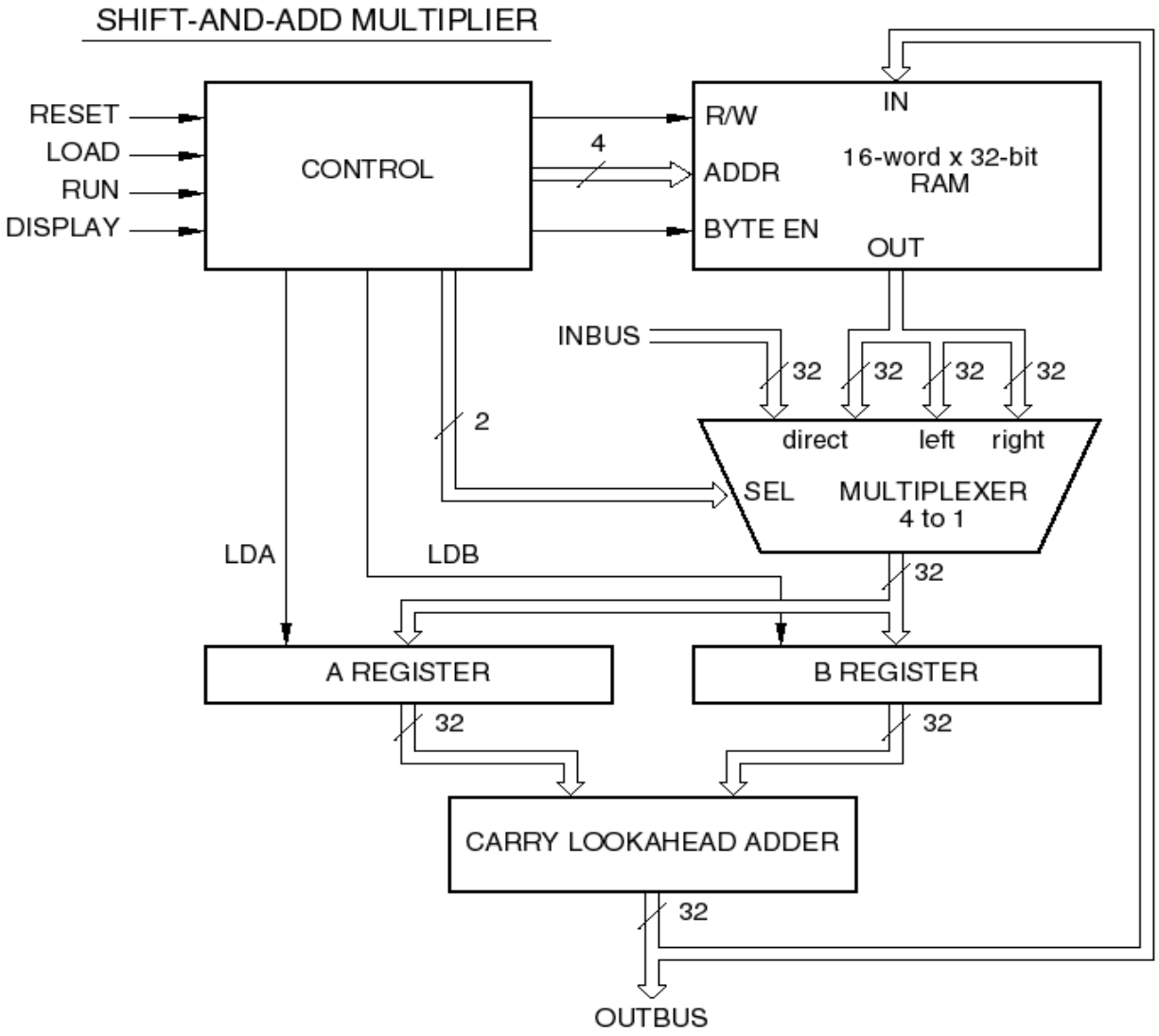
Suggested Reading

- Sections 5.1-5.2

Documentation Standards

- Block Diagrams
    - First step in hierarchical design
- Schematic Diagrams
-HDL Programs (ABEL, Verilog, VHDL)
- Timing Diagrams
- Circuit Descriptions

Block Diagram



Schematic Diagrams

-Details of component inputs, outputs, and interconnections

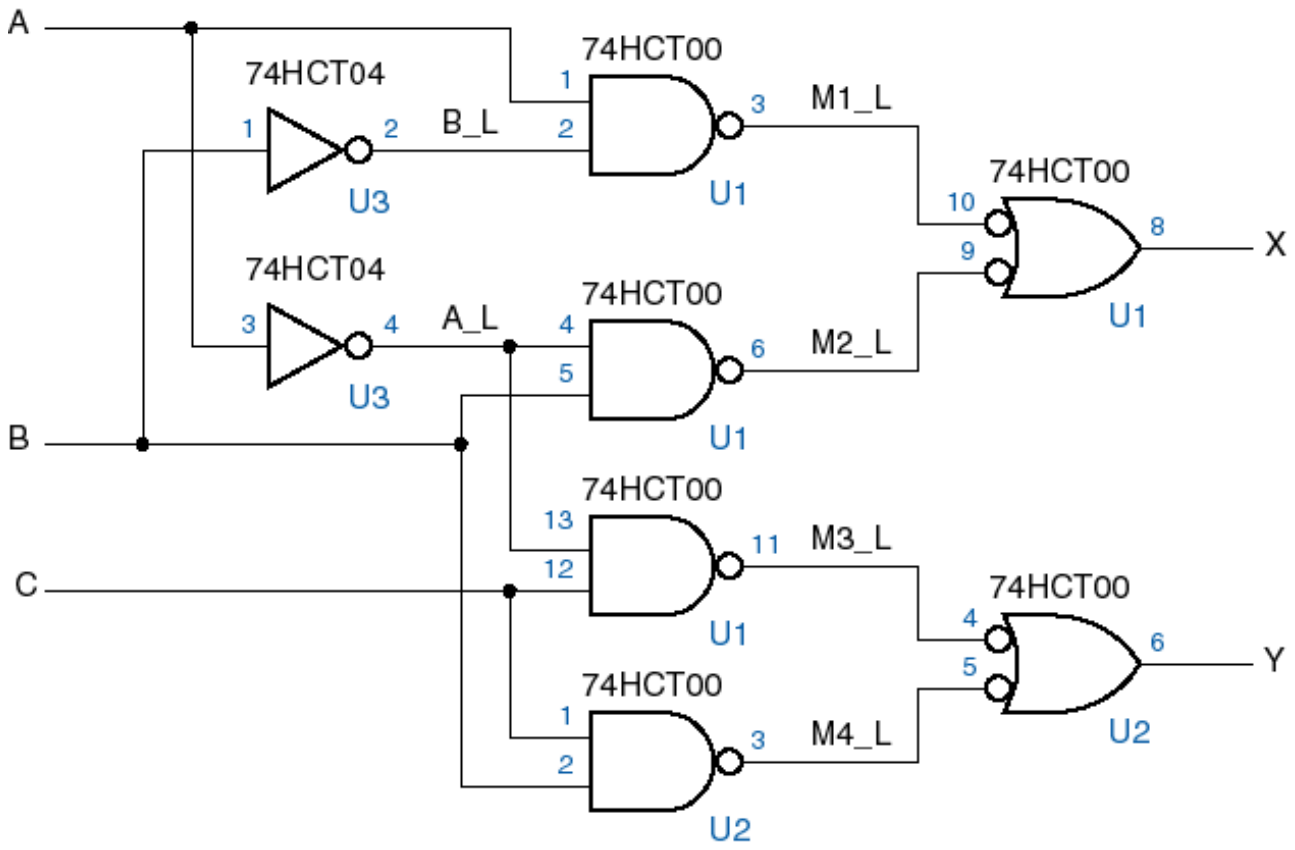
- Pin numbers

-Title blocks

-Names for all signals

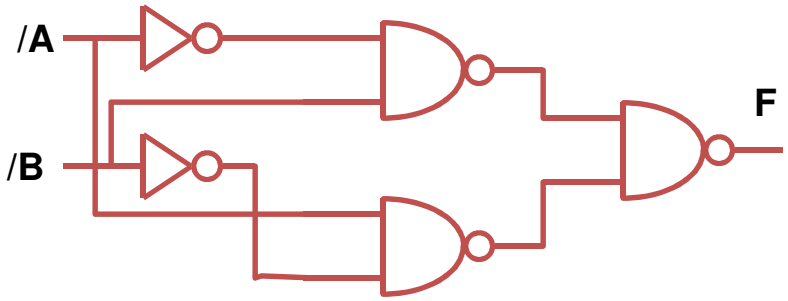
-Page-to-page connectors

Example Schematic

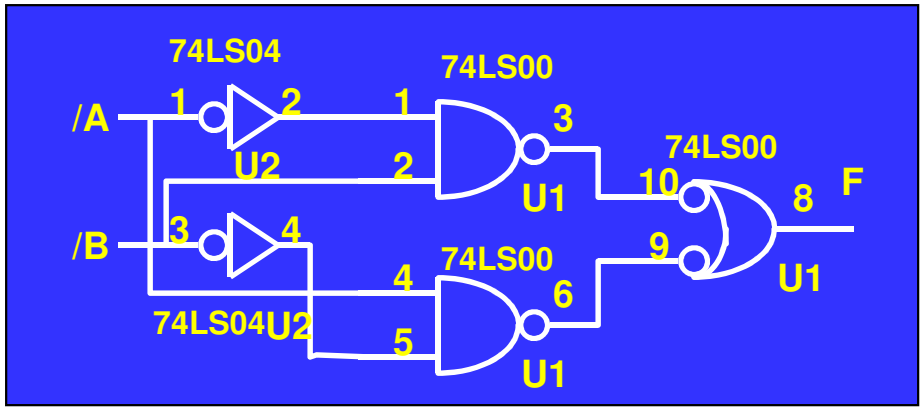


Schematic diagram/Logic Diagram

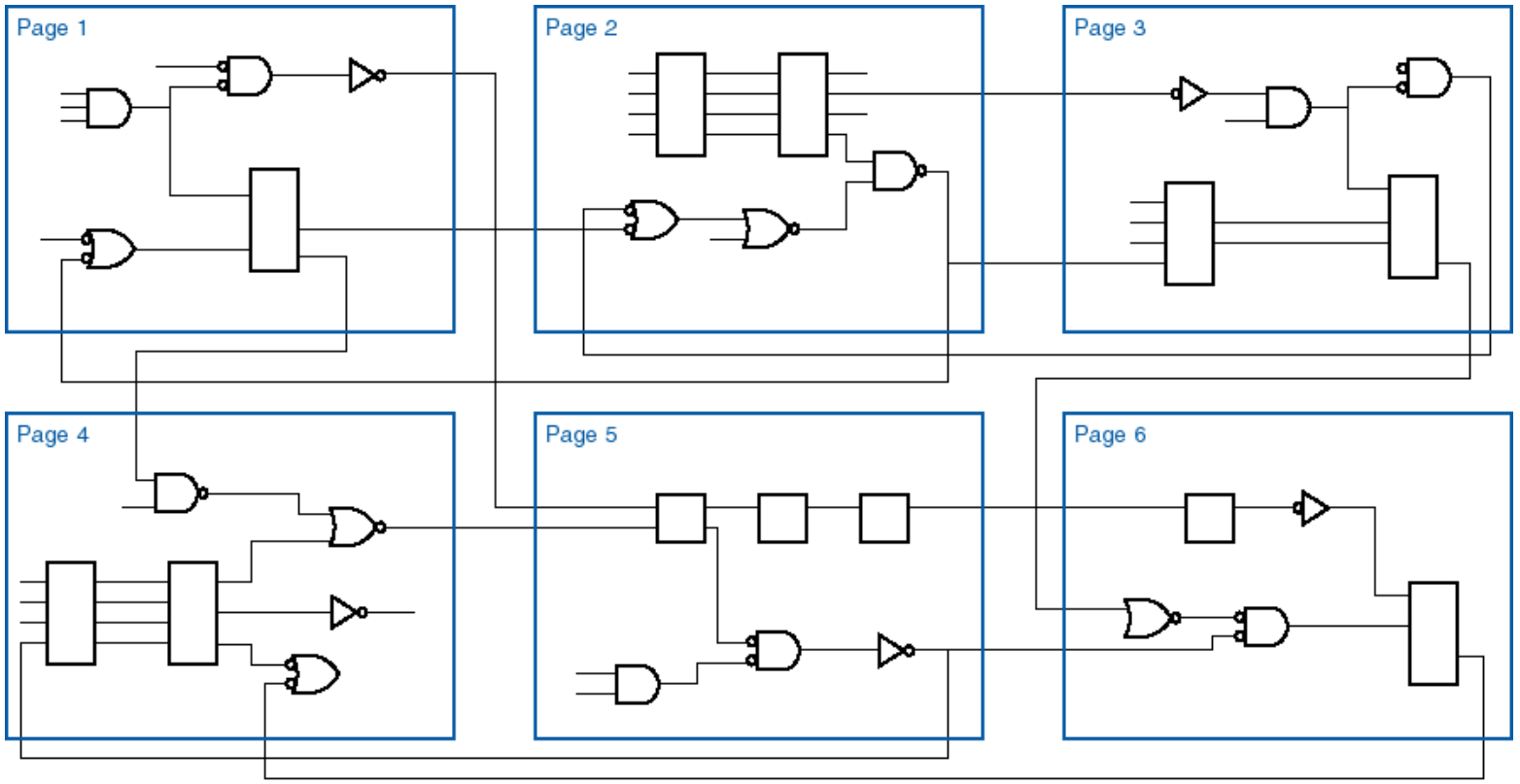
Logic Diagram



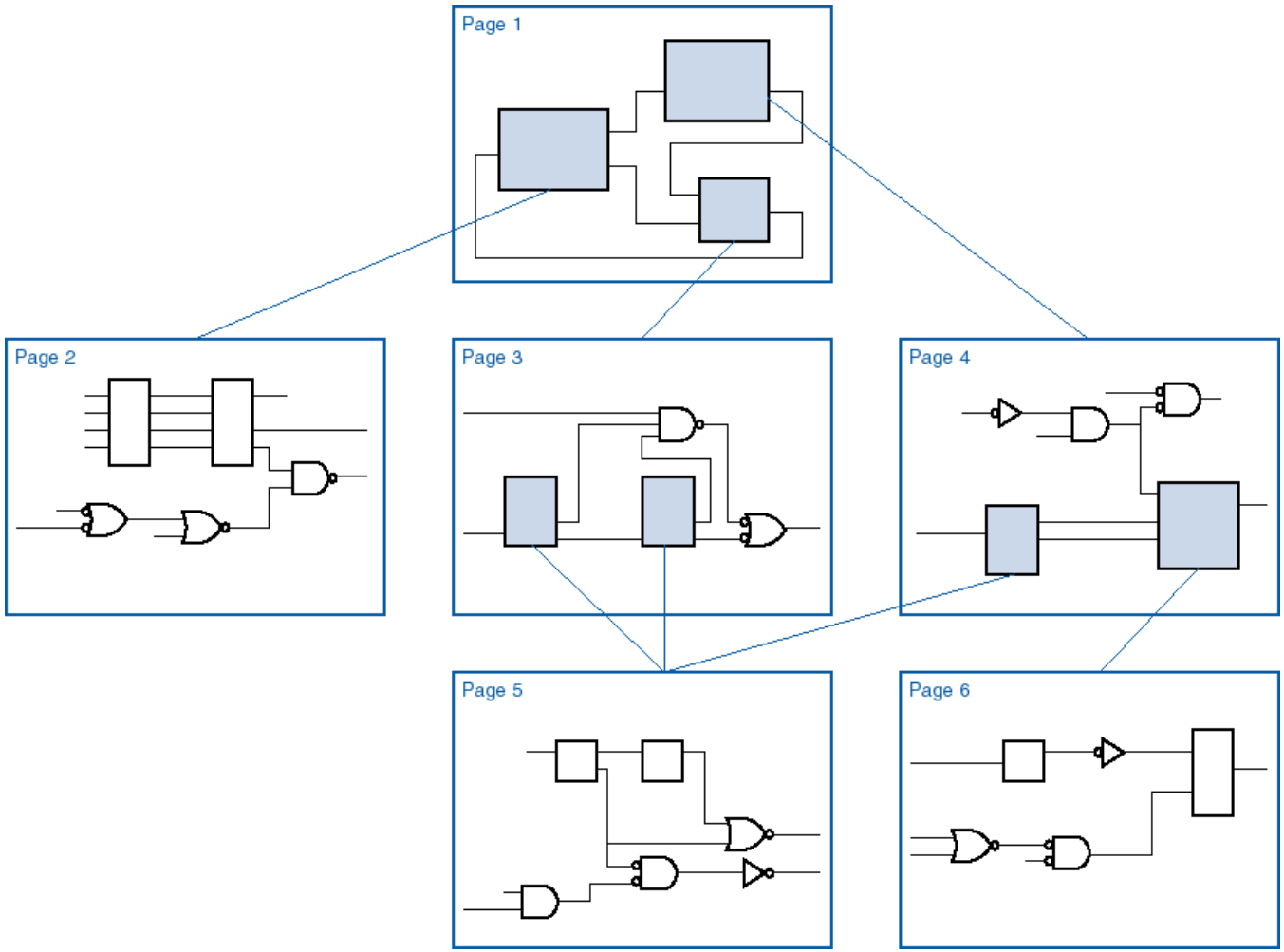
Schematic Diagram



Flat Schematic Structure



Hierarchical Schematic Structure



Other Documentation

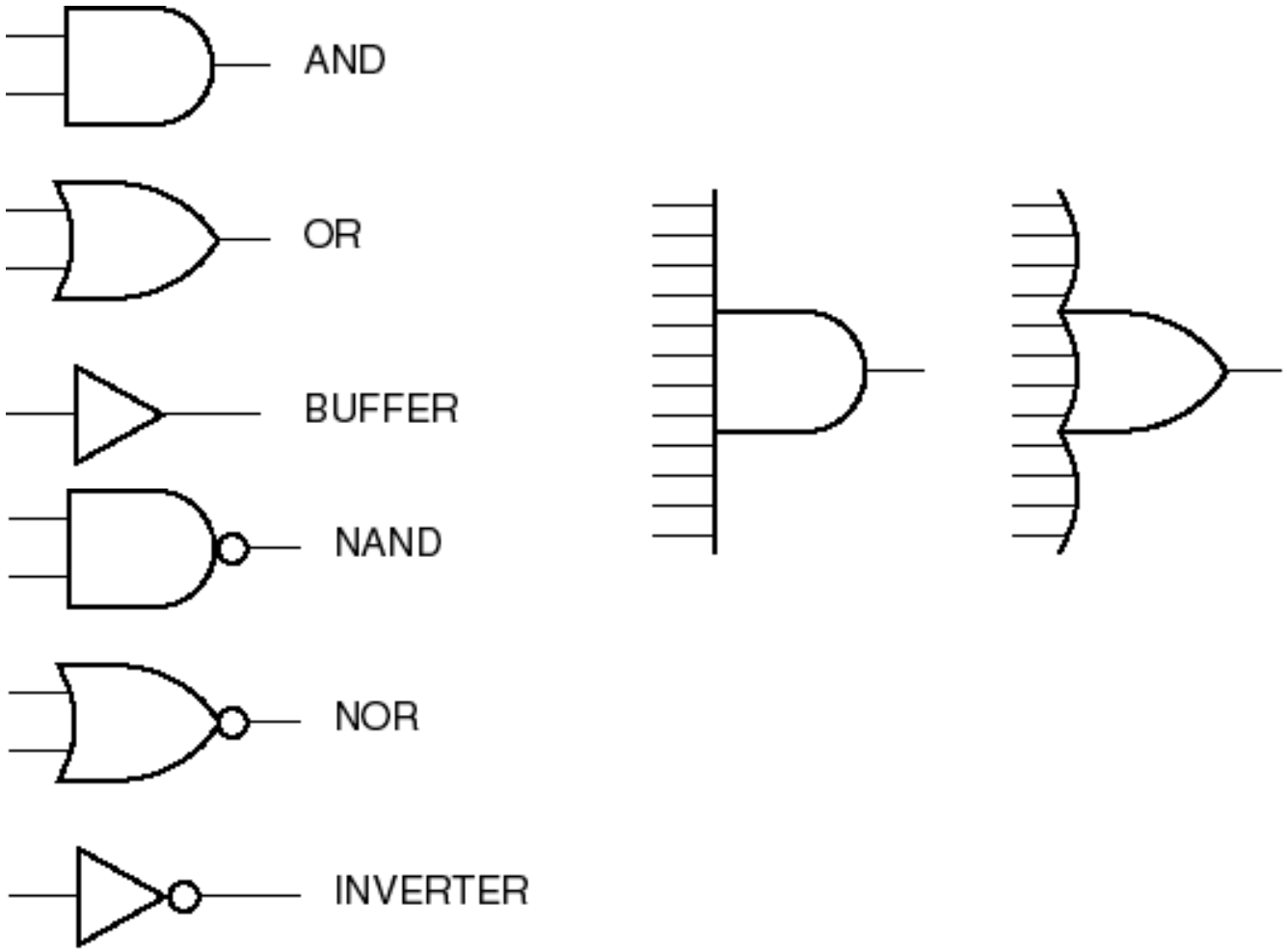
Timing diagrams

- Output from simulator
- Specialized timing-diagram drawing tools

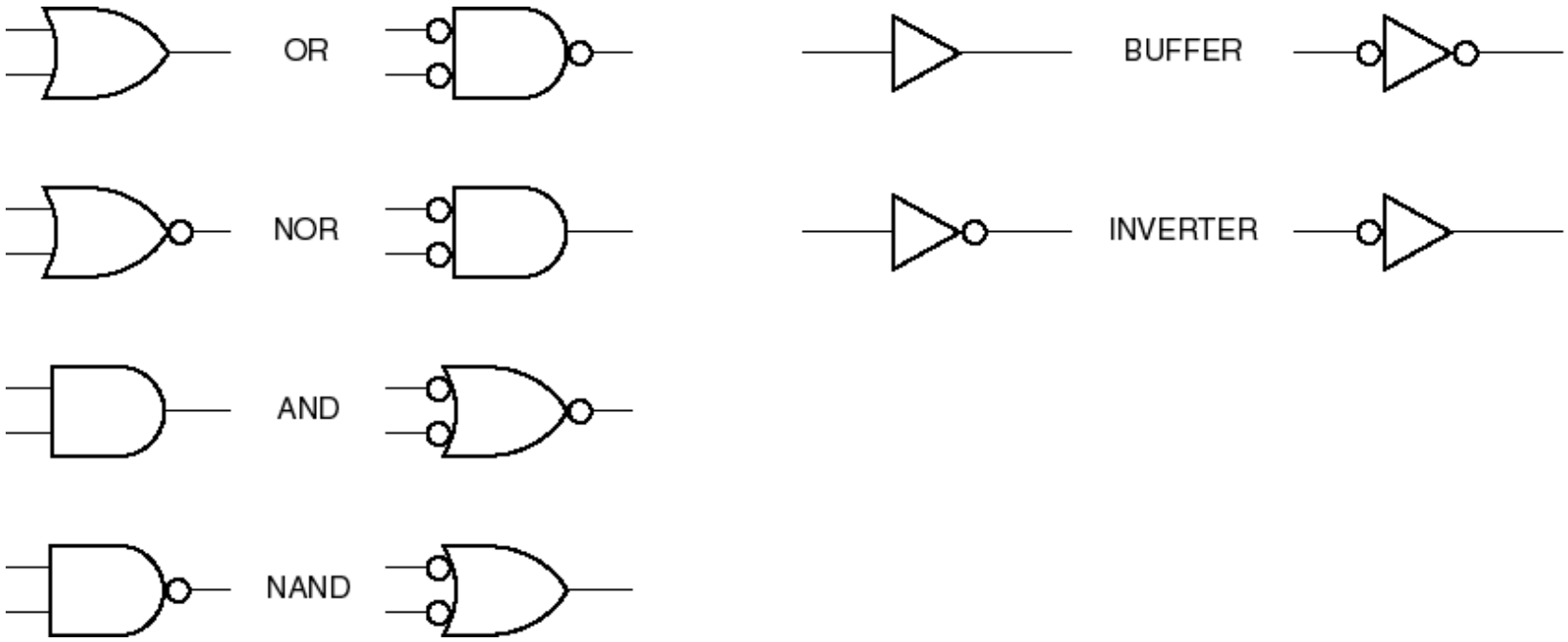
Circuit descriptions

- Text (word processing)
- Can be as big as a book (e.g., typical Cisco ASIC descriptions)
- Typically incorporate other elements (block diagrams, timing diagrams, etc.)

Gate Symbols



DeMorgan Equivalent Symbols



Which symbol to use?

Answer depends on signal **names** and **active levels**.

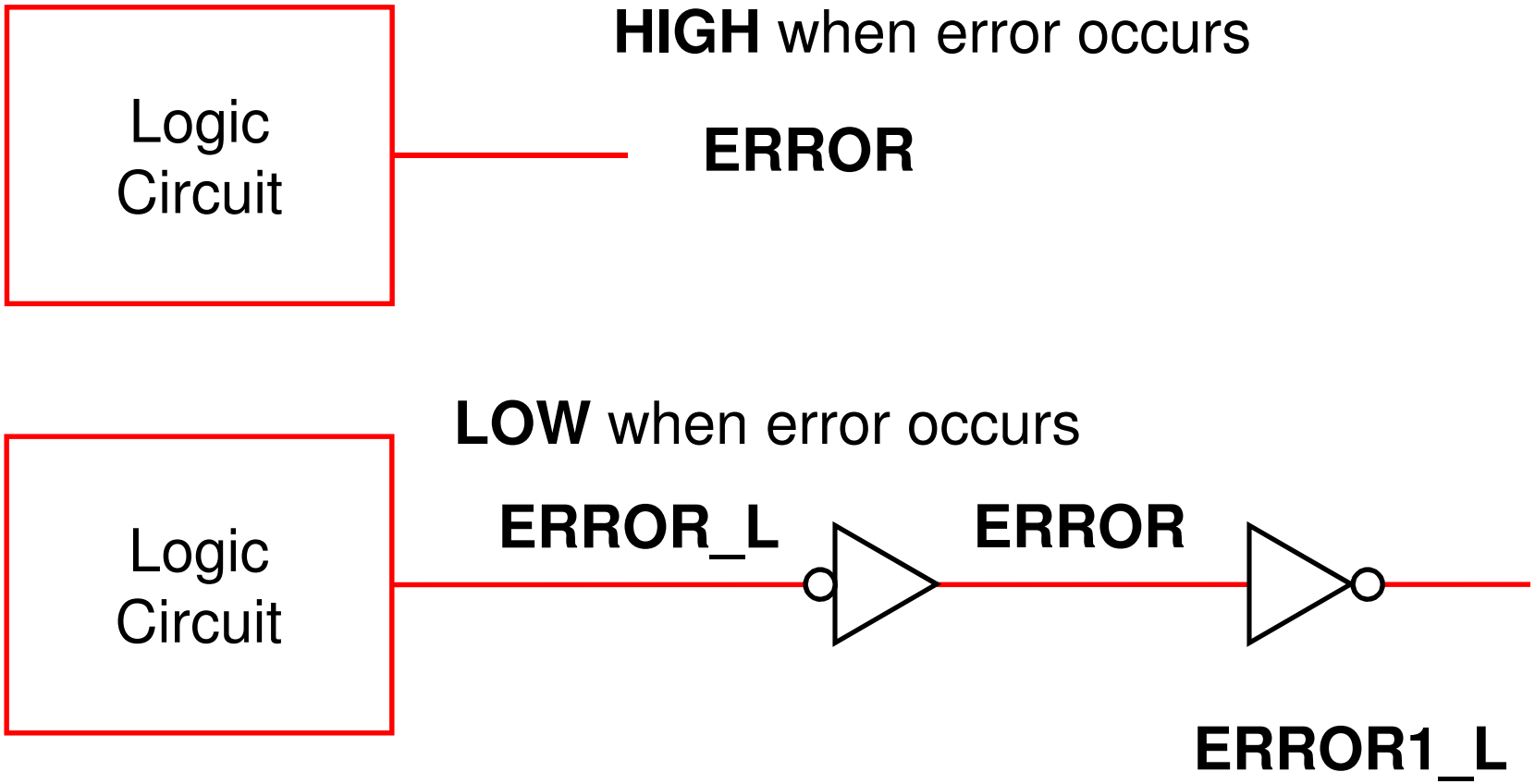
Signal Names and Active Levels

Signal names are chosen to be descriptive.

Active levels: HIGH or LOW

Active Low	*Active High*
READY–	READY+
ERROR.L	ERROR.H
ADDR15(L)	ADDR15(H)
RESET*	RESET
ENABLE~	ENABLE
~GO	GO
/RECEIVE	RECEIVE
TRANSMIT_L	TRANSMIT

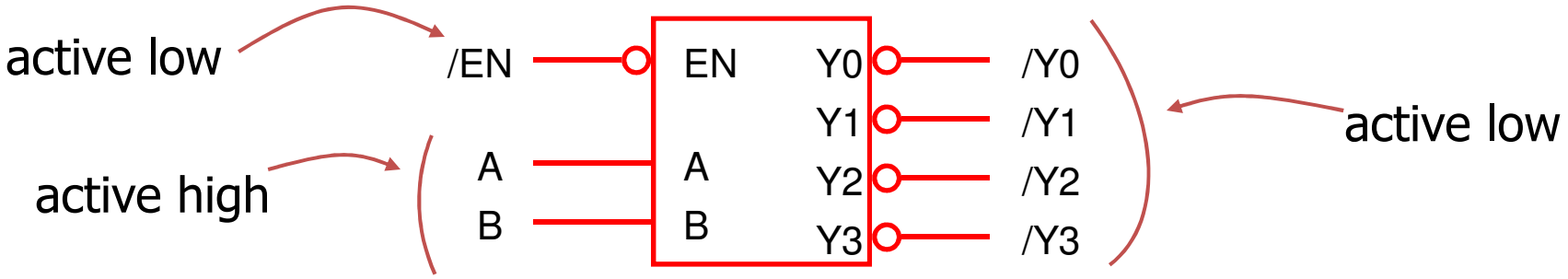
Example


Logic
Circuit
HIGH when error occurs
ERROR
Logic
Circuit
LOW when error occurs
ERROR_L
ERROR
ERROR1_L

Active Levels for Pins

In logic gates and logic structures the **inversion bubble** indicates the **active** level of the signal

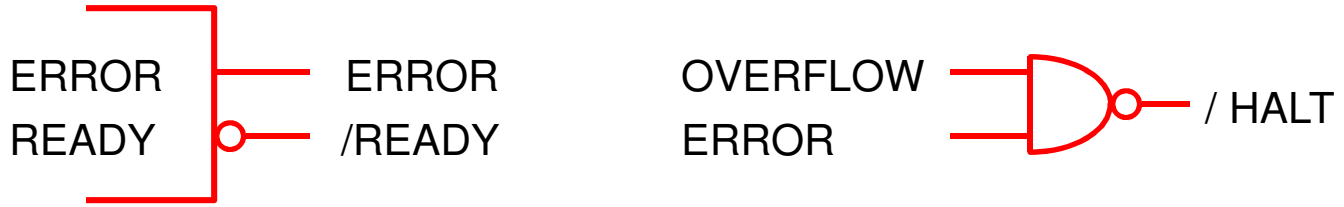
Examples: 2-to-4 Decoder



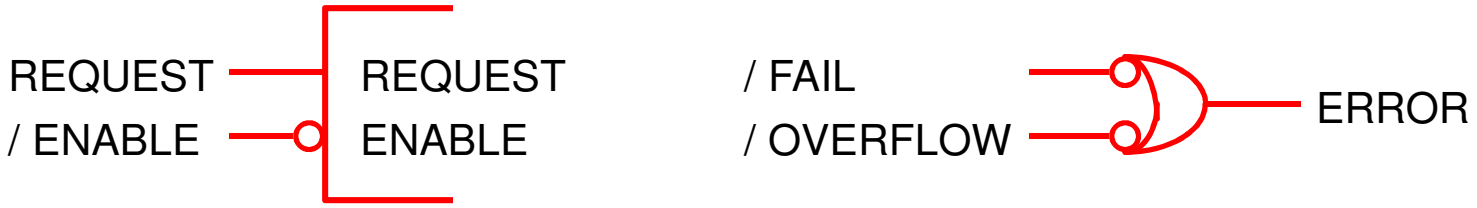
Bubble-to-Bubble Logic Design

Rules:

The active level of the **output signal** of a logic device should match the active level of the device's **output pin**.

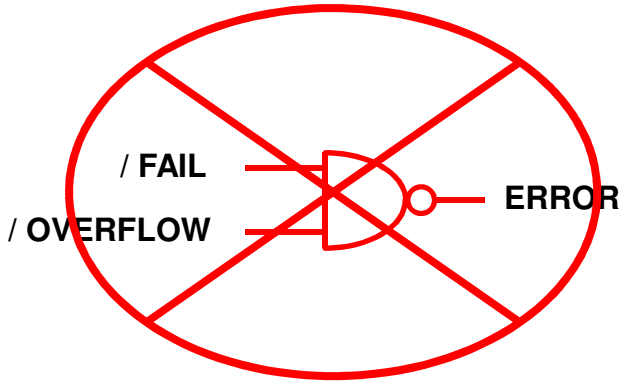


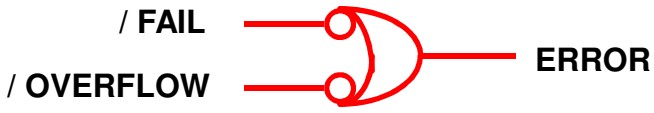
The active level of the **input signal** of a logic device should match the active level of the device's **input pin**.



Bubble-to-Bubble Logic Design

Purpose: To make it easy to understand the function of the Logic circuit





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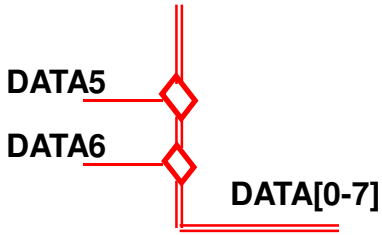
Drawing Layouts

Inputs to the left, outputs to the right. Signals flow from left to right.

Crossing lines/Connected lines (T-type connection)

Buses should be named: DATA[0-7], CONTROL

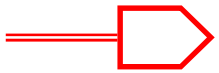
A signal extracted from a bus should be named



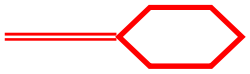
Broken signal paths should be flagged to indicate the source or destination and direction.

Bus Flags:

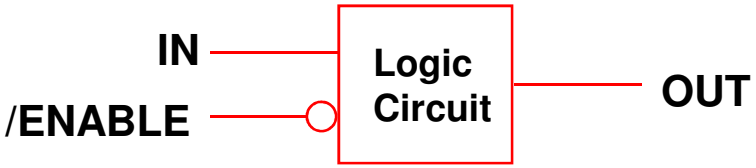
Unidirection

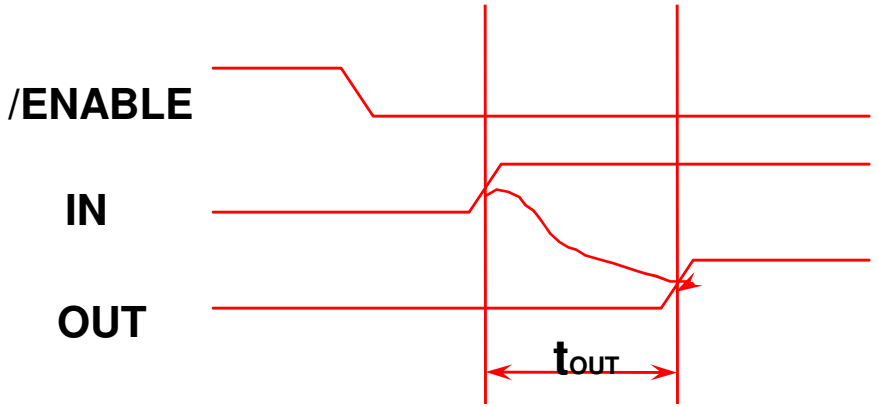


Bidirection



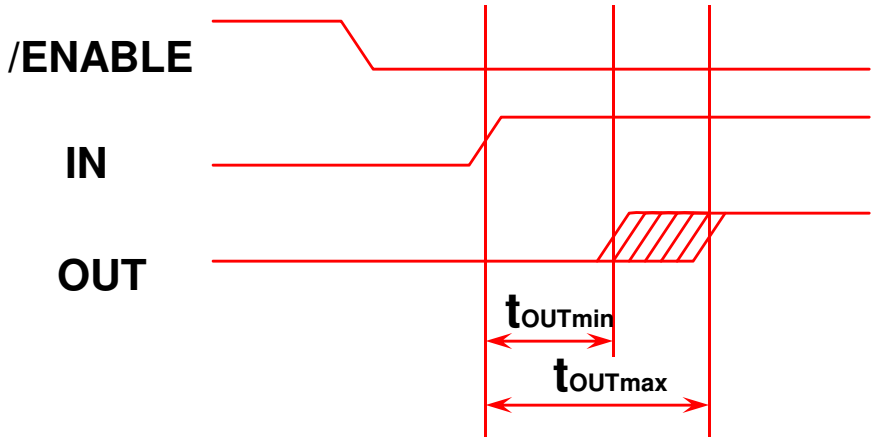
Timing Diagrams



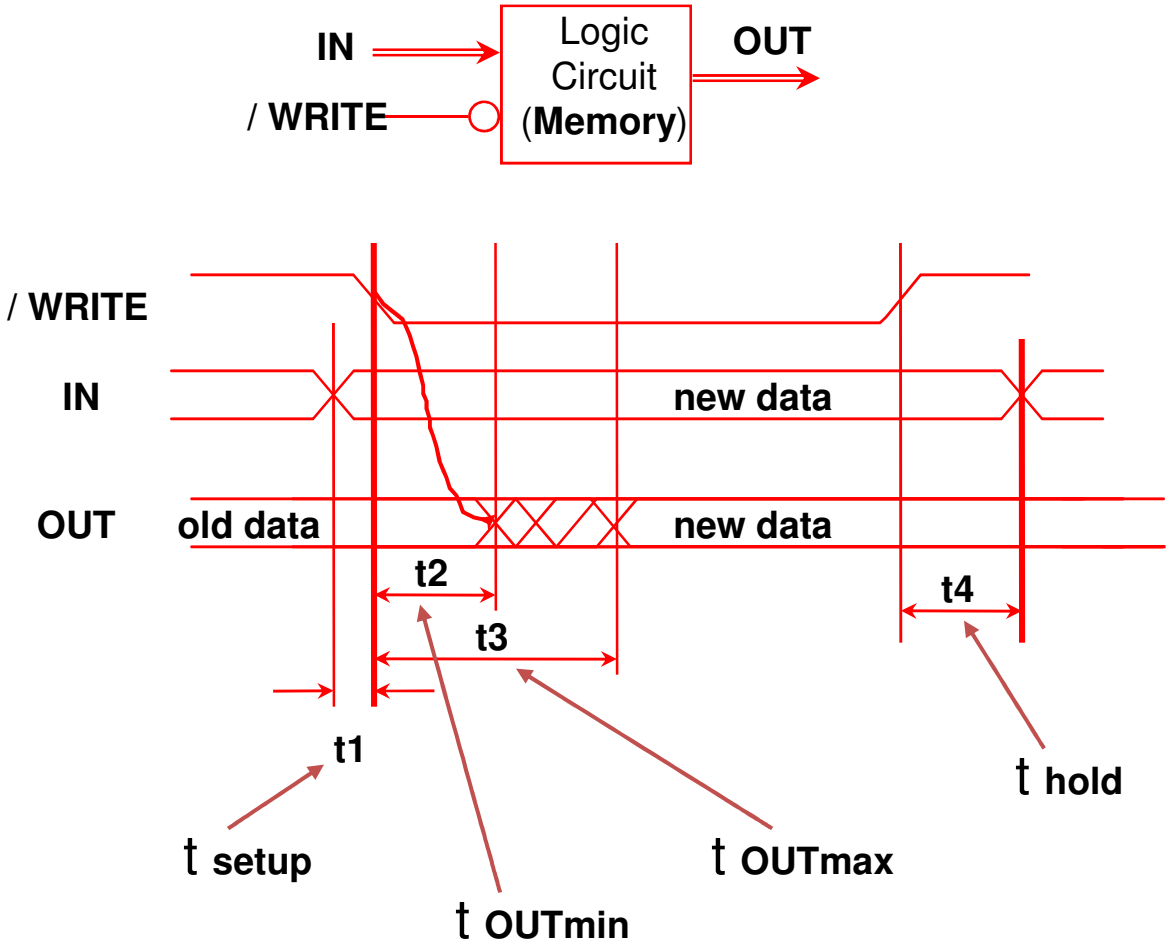


Delay depends on

- Internal circuit structure
- Logic Family type
- Source Voltage
- Temperature



Timing Diagram for Data Signals (Bus)



Propagation Delay

The Propagation Delay is the delay time between input transitions and the output transitions due to the propagation delay of the the logic gates

$\mathbf{t_p}$ of a signal depends on the signal path inside the logic circuit

To find $\mathbf{t_p}$ for a signal, add the propagation delays of all gates along the path of the signal

For a logic gate $\mathbf{t_{pLH}}$ may not equal $\mathbf{t_{pHL}}$

$\mathbf{t_p}$ is specified in the manufacturer data sheets of the IC's

Example:

	Typical (ns)		Maximum (ns)	
	t_{pLH}	t_{pHL}	t_{pLH}	t_{pHL}
74LS00	9	10	15	15
74ACT00	5.5	4.0	9.5	8.0