Faculty of Engineering

CSE115: Digital Design

Lecture 1: Introduction

SYNOPSYS®

These slides were created as part of the Synopsys Courseware Collection

Teaching Staff

- **Instructors:**
  - Dr. Maged Ghoneima
- **Assistants:**
  - Eng. Islam Azzam

Interaction

- I prefer dialogue in the class
- I like lots of questions
- If the questions lead us off track, we'll put them off until after class
- If I don't know, I'll tell you
- If it's relevant one of us will get the action to get the answer and report back
- Waiting to ask a question at the end is NOT a good strategy
  - May run short at the end
  - Learning best happens at the point when all of our minds are engaged on a topic
- "Teaching is an act of vulnerability" – I don't know the answers to all of your possible questions, but together we will try to find them

Course Characteristics

- This is not
  - A course to derive underlying mathematics
  - A course that teaches about one product
  - A course about tinkering
- This is a course intended
  - To introduce you to important concepts in a hands-on environment
  - To inspire a curiosity about why things work the way they do
  - To give you tools that you can use in later design courses
  - To help you develop your thinking as an engineer

Course Texts and Software

- Texts:
  - Class Notes
  - John F. Wakerly , Digital Design Principles and Practices – 3rd Ed, Prentice Hall (http://www.ddpp.com)
- Course Webpage:
  - http://mct.asu.edu.eg/cse115.html
- Circuit Simulator:
  - Synopsys Tools
  - or any other simulation tool you prefer and have access too

Grading

- 10% - Attendance & Assignments
- 10% - Quizzes & Class Contribution
- 10% - Labs
- 10% - Midterm Exam
- 25% - Project
- 40% - Final Exam

Academic Integrity

- Academic dishonesty is a very serious matter.
- Student-teacher relationships are built upon trust. Acts which violate this trust undermine the educational process.
- Any portion of work handed in that is not your own, should cite the author. The penalties for plagiarism and other forms of cheating can be quite harsh.
- Collaboration on assignments is encouraged, in fact essential, between lab partners. However, having one partner always work on hardware aspects and the other on the software or data analysis or report writing will be detrimental to all partners. All partners should understand and participate in all aspects of the lab exercise.
- Cheating on an exam will be considered as academic dishonesty and will result in a failing grade for the course.

Agenda

- Applications
  - Integrated Circuits
  - Computers
- Design Methodology
  - Bottom-up Analysis
  - Top-down Synthesis
- Course Outline

A Few Application Fields!

Communication

Computing

Aerospace

Health

Education

Home Electronics

Entertainment

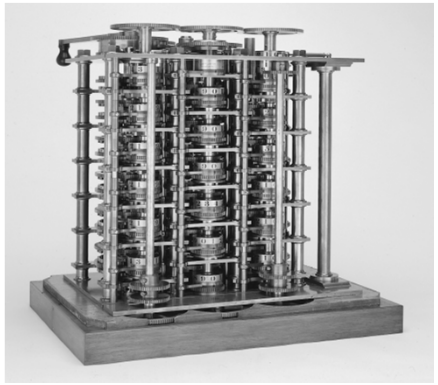
Aviation

Security

Automotive

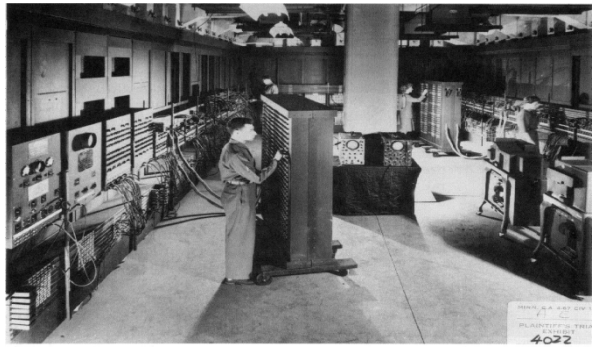
A Brief History of Computers

Babbage Difference Machine

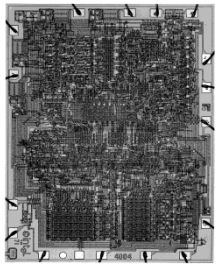


1831: The First Computer
25,000 parts

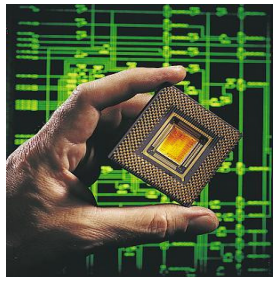
ENIAC

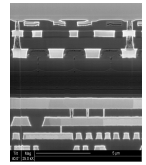


1946: The First Electronic Computer
17,000 vacuum tubes. **5,000 additions/sec**



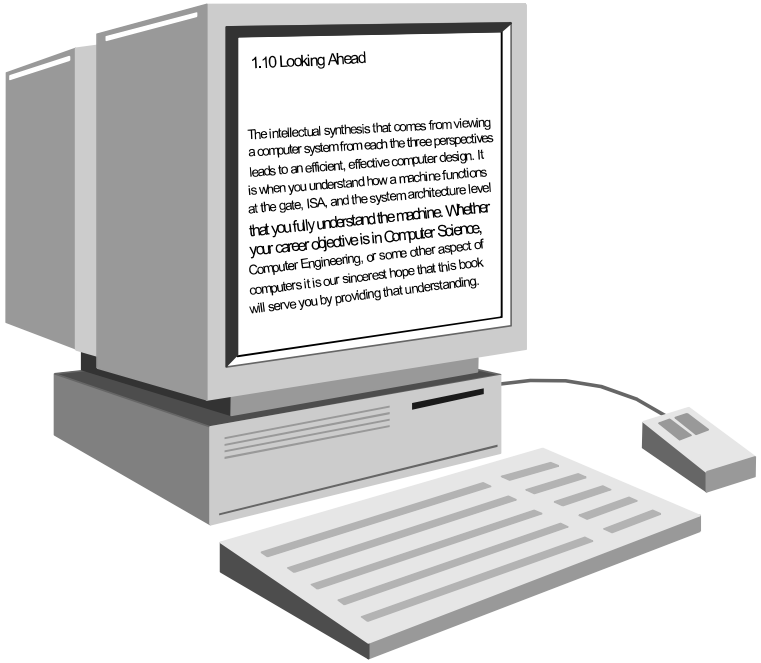
1971: Intel 4004
2,300 Transistors
60,000 calculations/sec





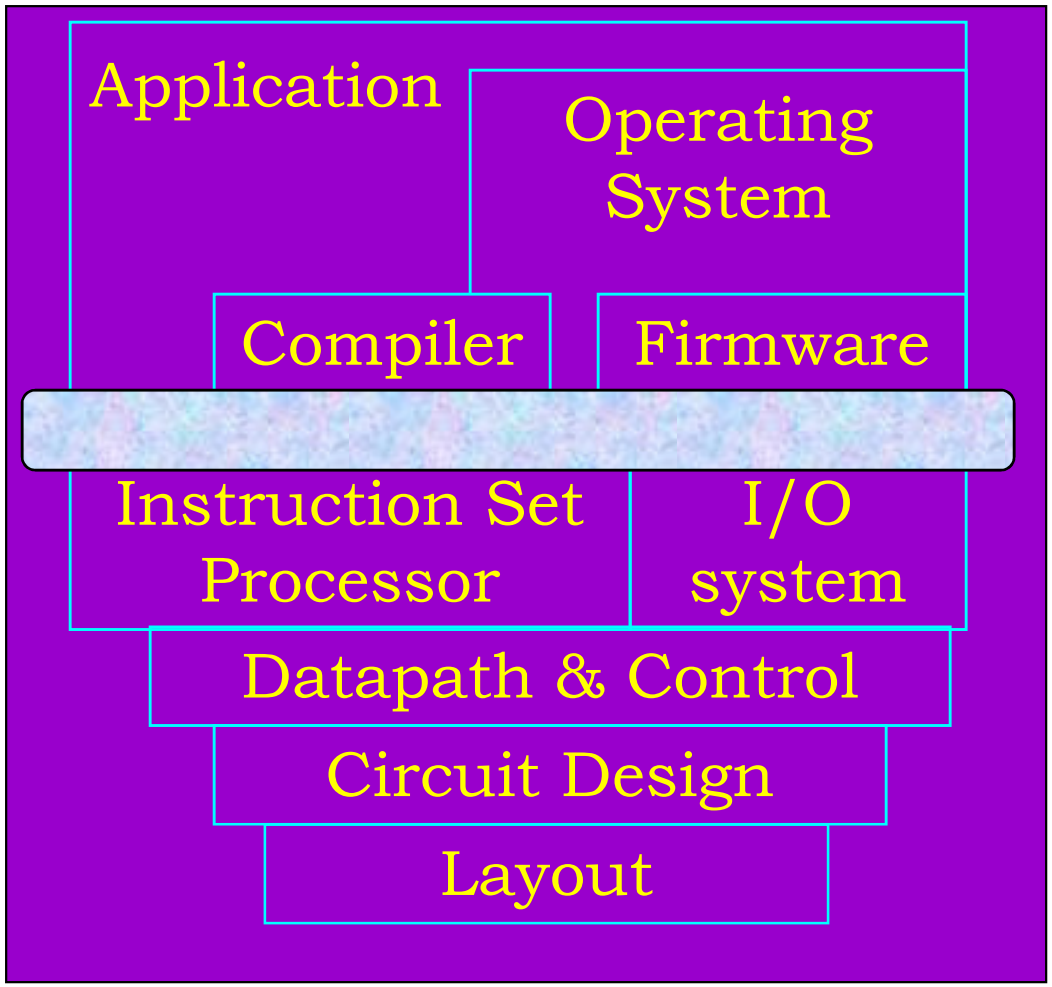
2007: Intel Itanium
77 Million Transistors
100 Million calculations/sec

Computers from Outside

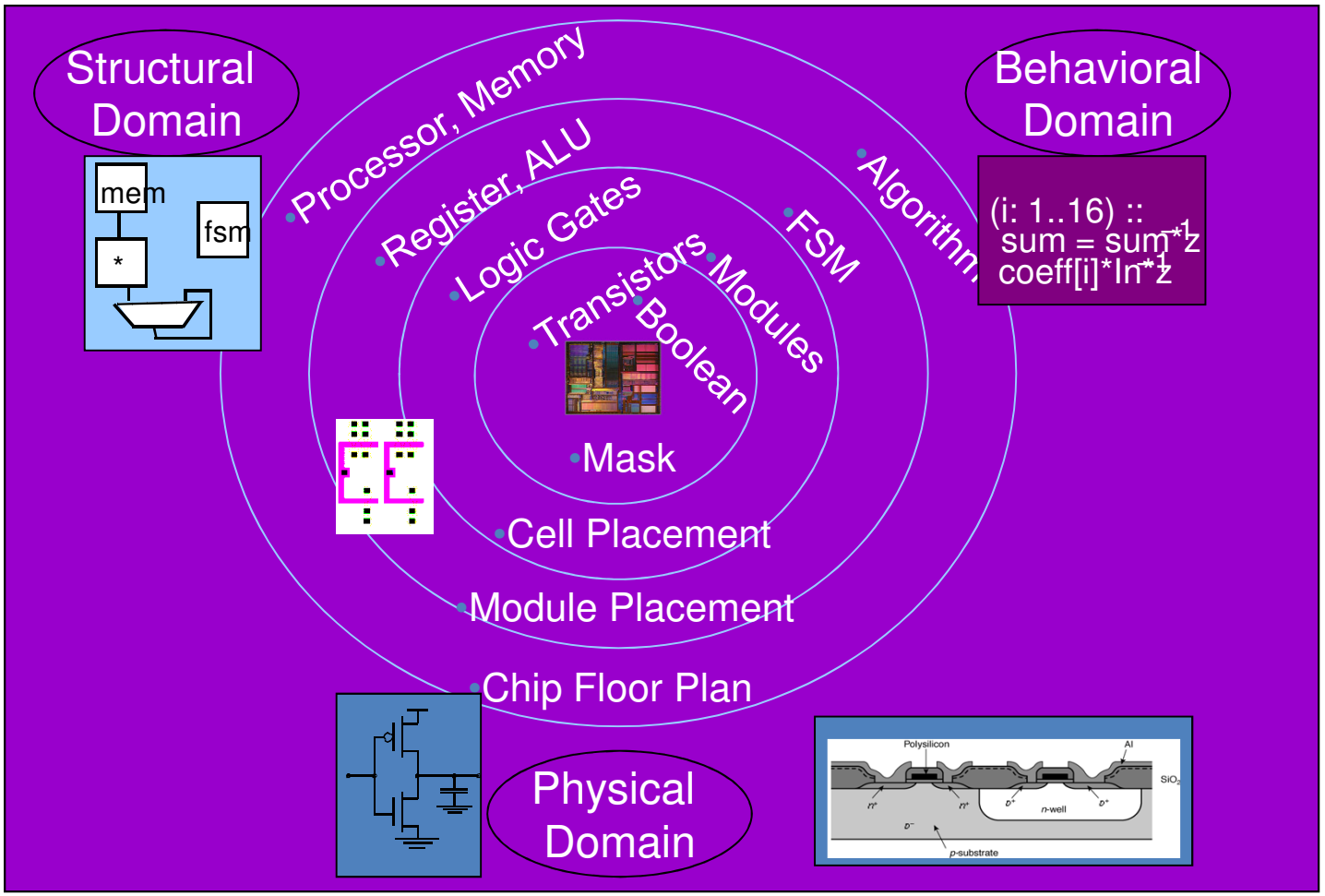


- Software
- Peripherals
- Speed
- Storage
- Cost

Computer Architecture



Chip design at the Crossroads



Use Existing Blocks: Synthesis

SYNOPSYS

A suite of state-of-the-art system design tools

Specification

Refinement

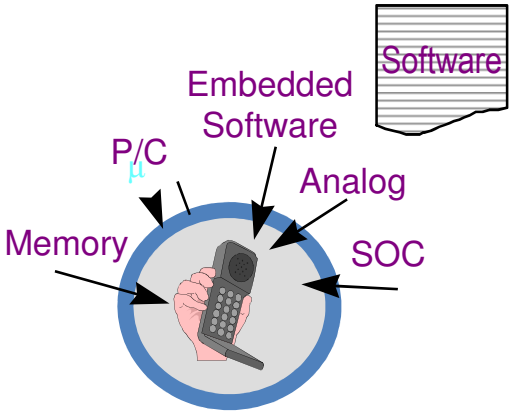
Implementation

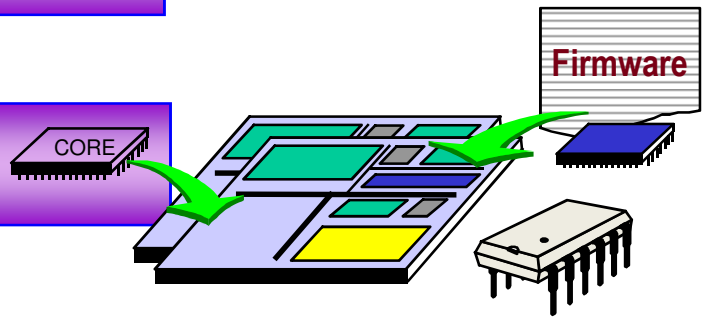
Chip level design planning

Block level implementation

Chip integration

Cell Route





Methodology

Top-down design – ***Design complex circuits in a simple way***

Architecture

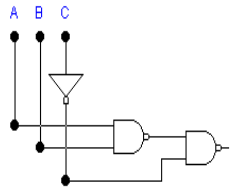
Components

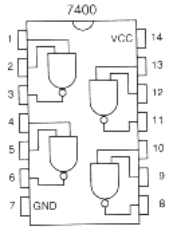
Gates

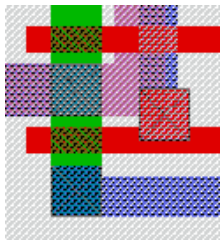
Transistors

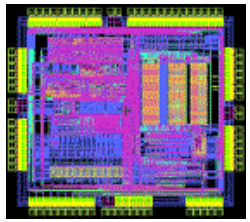
Layout

IC









F=AB+C

Bottom-up analysis – Analyze simple components in a complex way

Course Outline

- **Number Systems and Codes**: (3 weeks)
  - Binary, Octal, and Hex Radices; Addition, Subtraction.
  - Conversion between Radices; Two's Complement; Other Codes.

- **Combinational Logic Design Principles:** (4 weeks)
  - Switching Algebra, Combinational Circuit Analysis, Synthesis and Minimization, Karnaugh Maps, Timing Hazards.

- **Combinational Logic Design Practices:** (3 weeks)
  - Drawing Standards.
  - Decoders, Three-State Buffers, Encoders, Multiplexers, Exclusive OR, Comparators, Adders, Subtracters and ALUs.

Course Outline (2)

- **Sequential Logic Design Principles and Practices:** (5 weeks)
  - S-R, J-K, D and T flip-flops, Master Slave Configuration, Latches.
  - Analysis of State Machines, State Tables, State Minimization, State Assignment and Synthesis.
  - Synchronous System Timing
  - Latches, Flip-flops, and Registers
  - Counters
  - Shift Registers