

Sheet 2, Verilog & Logic Design

1. Write three different descriptions of a full adder. One description should use gate-level models, another should use continuous assignment statements, and the third should use combinational always.
2. Draw the wave diagram of the *clock* generated by the following module:

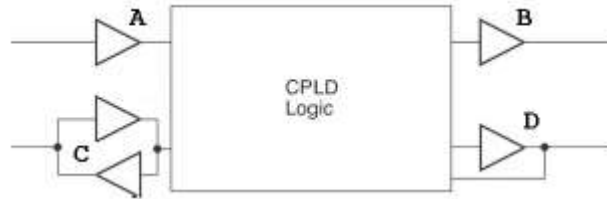
```
module m555 (clock);  
    output    clock;  
    reg clock;  
  
    initial  
        #5 clock = 1;  
  
    always  
        #50 clock = ~clock;  
endmodule
```

3. Change the module m555 (of the previous problem) such that the clock period remains the same but the *duty cycle* becomes 40%.
4. Write a two phase clock generator. Phase 2 should be offset from phase 1 by one quarter of a cycle.
5. Keeping the same output timing, replace the initial and always statements in the module m555 with gate primitives.
6. Here's a Verilog module that is complete except for the *register*, *input*, and *output* declarations. What should they be? Assume *a*, *b*, and *c* are 8-bit "things" and the others are single bit. Note that you may have to add to the input/output list. Do not add any more assignments (only input, output, and register declarations).

```
module silly (a,b,c,q, ...);  
    // oops, forgot the declarations!  
    initial  
        q = 1'b0;  
  
    always  
        begin  
            @(posedge y)  
                #10 a = b + c;  
            q = ~q ;  
        end  
    nand #10 (y,q,r) ;  
endmodule
```

7. Choose the right answer

- a. The idea behind signal concurrency is that all signals in a simulation are executed at _____.
A. a fixed time B. the same time C. a predetermined time D. Eastern-Daylight Time.
- b. Which of the following is an invalid name in Verilog?
A. DECODE8 B. _WHAT_4 C. \$INVALID D. All are valid
- c. A digital circuit designed to detect the presence of a particular digital state is called:
A. Multiplexer B. Decoder C. Parity Generator D. Encoder
- d. A circuit that generates a binary code at its outputs in response to one or more active input lines.
A. Encoder B. Decoder C. Demultiplexer D. Shift-Register
- e. Which of the following best represents the INOUT mode?



- f. A circuit that uses a binary decoder to direct a digital signal from a single source to one of several destinations.
A. Decoder B. Multiplexer C. Demultiplexer D. Parity Generator
 - g. An error-checking system that requires a binary number to have an even number of 1s.
A. Even Parity B. Parity C. Odd Parity D. Multiplexer
8. Write a Verilog code for a D-type f/f with synchronous reset.
9. Write a Verilog code for a D-type f/f with asynchronous reset.
10. Assume $A = "0011"$, $B = "011"$, $C = "101"$, what will be the result of the following statements:
- a. $A + (B|C)$
 - b. $\sim\&A$
 - c. $(A == B) ? B : C$
 - d. $\{A, \{2\{C\}\}$