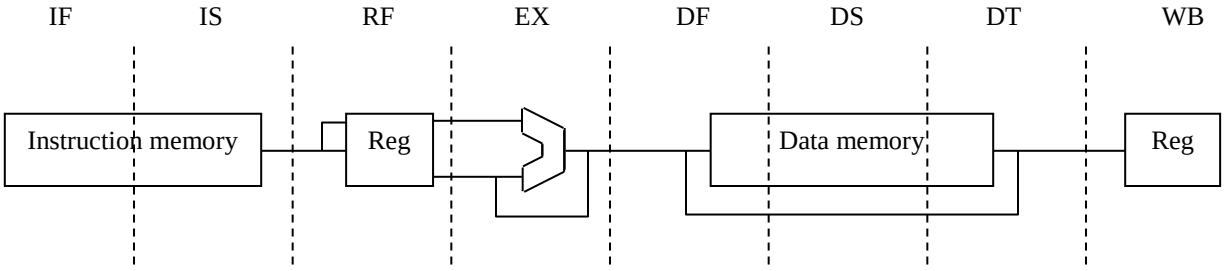
Mechatronics Department
Computer Organization, CSE315
Third Year – 2014/2015

Sheet 6, Pipelines

1. Assume a pipelined machine of 5 stages. Each stage has a delay of 5 ns. What is the time required to execute an instruction in an unpipelined machine. In the piplined version, what is the time required to execute 1 instruction, 2 instructions, 3 instructions … etc. Draw a curve showing the speedup versus the number of instruction executed.

2. Suppose that 30% of the instructions are loads. In 50% of the cases, an instruction that follows a load instruction depends on the result of the load. If this hazard creates a single-cycle delay, how much faster is the ideal pipelined machine?

3. Consider the pipeline structure of the MIPS R4000 processor (a variant of MIPS) shown below. This pipeline has 8 stages as shown below:



IF: First half of instruction fetch
IS: Second half of instruction fetch
RF: Instruction decode and register fetch
EX: Execution
DF: First third of data fetch
DS: Second third of data fetch
DT: Last third o data fetch
WB: Write back

Show how the following program advances in the pipeline, by filling the pipeline timing chart shown below.

```
lw      R1,10(R5)       ;load R1 with the content of the memory location 10 + R5
add     R2,R2,R1        ;load R2 with the content of the R1 + R2
```

```
sub     R3,R3,R1        ;load R3 with the content of the R3 + R1
or      R4,R4,R1        ;load R4 with the content of the R4 OR R1
```

For each instruction, write the name of the pipeline stage used at every cycle.

	Cycle number														
	1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**
Lw R1,10(R5)															
add R2,R2,R1															
sub R3,R3,R1															
Or R4,R4,R1															

4. "Increasing the number of pipeline stages always increases performance". Discuss this statement.

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