Mechatronics Department
Computer Organization, CSE315
Third Year – 2014/2015

Sheet 4, Register Transfers

Question 1:
Show the block diagram of the hardware that implements the following register transfer statement:

yT_2: $R_2 \leftarrow R_1$, $R_1 \leftarrow R_2$

Question 2:
The outputs of four registers R_0, R_1, R_2, and R_3 are connected through 4-to-1 multiplexer to the inputs of a fifth register R5. Each register is eight bits long. The required transfers are dictated by four timing variables T0 through T3 as follows:

T_0: $R_5 \leftarrow R_0$
T_1: $R_5 \leftarrow R_1$
T_2: $R_5 \leftarrow R_2$
T_3: $R_5 \leftarrow R_3$

The timing variables are mutually exclusive, which means that only one variable is equal to 1 at any time, while the other three are equal to 0. Draw a block diagram showing the hardware implementation of the register transfers. Include the connections necessary from the four timing variables to the selection inputs of the multiplexer and to the load input of the register R_5.

Question 3:
Represent the following conditional control statement by two register transfer statements with control functions.

If (P=1) then ($R_1 \leftarrow R_2$) else if (Q=1) then ($R_1 \leftarrow R_3$)

Question 4:
A digital computer has a common bus system for 16 registers of 32 bits each. The bus is constructed with multiplexers.

a. How many selection inputs are there in each multiplexer?
b. What size of multiplexers is needed?
c. How many multiplexers are there in the bus?

Question 5:
The following transfer statements specify a memory. Explain the memory operation in each case.

a. $R_2 \leftarrow M[AR]$
b. $M[AR] \leftarrow R_3$
c. $R_5 \leftarrow M[R5]$

Question 5:
Draw the block diagram for the hardware that implements the following statement:

$x + yz$: $AR \leftarrow AR + BR$

Where AR and BR are two n-bit registers and x, y, and z are control variables. Include the logic gates for the control function.

Question 6:

Show the hardware that implements the following statement. Include the logic gates for the control function and a block diagram for the binary counter with a count enable input.

$xyT_0 + T_1 + Y'T_2$: $AR \leftarrow AR + 1$

Question 7:

Consider the following register transfer statements for two 4-bit registers R_1 and R_2

xT: $R_1 \leftarrow R_1 + R_2$
$x'T$: $R_1 \leftarrow R_2$

Every time that variable T = 1, either the content of R_2 is added to the content of R_1 if x = 1, or the content of R_2 is transferred to R_1 if x = 0. Draw a diagram showing the hardware implementation of the two statements.

Question 8:

Design an arithmetic circuit with one selection variable S, and two n-bit data inputs A and B. The circuit generates the following four arithmetic operations in conjunction with the input carry Cin. Draw the logic diagram.

S	C_{in} = 0	C_{in} = 1
0	D= A plus B	D = A plus 1
1	D = A – 1	D = A plus B' plus 1

Question 9:

Design a digital circuit that performs the four logic operations of XOR, XNOR, NOR, and NAND. Use two selection variables.

Question 10:

Register A holds the b-bit binary 11011001. Determine the operand B and the logic micro-operation to be performed in order to change the value in A to:

a. 01101101
b. 11111101

Question 11:

The 8-bit registers Ar, BR, CR, and DR initially have the following values:

AR = 11110010
BR = 11111111
CR = 10111001
DR = 11101010

Determine the 8-bit values in each register after the execution of the following sequence of micro-operations.

$AR \leftarrow AR$ plus BR
$CR \leftarrow CR \wedge DR$, $BR \leftarrow BR$ plus 1
$AR \leftarrow AR - CR$

Question 12:

What is wrong with the following register transfer statements?

a. xT: $AR \leftarrow AR'$, $AR \leftarrow 0$
b. yT: $R1 \leftarrow R2$, $R_1 \leftarrow R_3$
c. zT: $PC \leftarrow AR$, $PC \leftarrow PC + 1$